Advances in Very High Frequency Power Conversion

Kovacevic, Milovan

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Milovan Kovacevic

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This report was prepared by
Milovan Kovacevic

Supervisors
Michael A.E. Andersen
Arnold Knott

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Department of Electrical Engineering
Electronics Group (ELE)
Technical University of Denmark
Oersteds Plads bygning 349
DK-2800 Kgs. Lyngby
Denmark

www.ele.elektro.dtu.dk
Tel: (+45) 45 25 25 25
Fax: (+45) 45 88 01 17
E-mail: elektro@elektro.dtu.dk

Preface and Acknowledgment

The PhD thesis titled *"Advances in Very High Frequency Power Conversion"* has been carried out at the Electronics group, Department of Electrical Engineering, Technical University of Denmark (DTU) during the period November 2011 to February 2015. The PhD project was co-funded by Danish Lighting Innovation Network, Copenhagen, Denmark, and FINsix Corporation in Menlo Park, California, where external research visit was carried out.

It is a matter of great pleasure and privilege to be able to express deep gratitude to all who stood by me and helped me throughout the project. Most of all:

- My PhD supervisors, Prof. Michael A. E. Andersen and Assoc. Prof. Arnold Knot, for providing me an opportunity to approach, and expand, the very boundaries of our understanding of power electronics. Their unwavering support, insightful suggestions, encouragement, and innumerable fruitful discussions throughout my PhD. Their advice on the subjects of power electronics was immensely helpful in carrying out my research.

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- Finally, I express my gratitude to all those who helped me directly or indirectly in the successful completion of my PhD.

Abstract

Resonant and quasi-resonant converters operated at frequencies above 30 MHz have attracted special attention in the last two decades. Compared to conventional converters operated at ~100 kHz, they offer significant advantages: smaller volume and weight, lower cost, and faster transient performance. Excellent performance and small size of magnetic components and capacitors at very high frequencies, along with constant advances in performance of power semiconductor devices, suggests a sizable shift in consumer power supplies market into this area in the near future.

To operate dc-dc converter power devices at very high frequencies, switching loss needs to reduced or eliminated, as it would become prohibitively large. In addition, as the frequency increases, hard-switched gate driving becomes less and less of an option, as it embodies the same loss mechanism. A low-loss gate drive methods may need to be applied, especially at low power levels where gating loss becomes a significant percentage of the total loss budget. Various resonant gate drive methods have been proposed to address this design challenge, with varying size, cost, and complexity. This dissertation presents a self-oscillating resonant gate drive solution, which is applicable in cases when there are at least two power stages, and with minimal additional hardware requirements. It is experimentally confirmed that the method is suitable for both parallel and serial input configurations. Compared to state-of-the-art solutions, the proposed method provides low complexity and low gate loss simultaneously. A direct design synthesis method is provided for resonant SEPIC converters employing this technique. Most experimental prototypes were developed using low cost, commercially available power semiconductors.

Due to very fast transient response of VHF converters, on/off control schemes are often used for their output control. The options presented so far demonstrated excellent performance, but with very strict timing constraints on all functional blocks in the feedback loop. Therefore, an on/off control method is proposed which allows the use of conventional ICs, while still providing high control bandwidth and performance comparable to state-of-the-art solutions.

Since in many applications of interest galvanic isolation is not a requirement, the thesis proposes a method for providing a DC power path from input to output of a previously galvanic isolated converter. The method requires connection rearrangement in the existing converter only, and provides higher output power and converter efficiency for the same or lower voltage and/or current stresses in the converter components.

Achieved results demonstrated that low-cost solutions, based on silicon power semiconductors and ICs, can achieve formidable performance even when operated at very high frequencies. The power devices employed in this thesis were not optimized for such operation. With proper optimization and new semiconductor materials, it is expected that VHF converters become frequent occurrence within the power conversion domain, rather than a curiosity.

Keywords: on/off control, very high frequency, dc-dc power conversion, resonant converters, switch-mode power supplies, zero-voltage switching

Resumé

Resonante og quasi resonante konvertere med skifte frekvenser over 30 MHz har tiltrukket stor opmærksomhed inden for de sidste to årtier. Sammenlignet med konventionelle konvertere med skifte frekvenser omkring ~100 KHz udmærker de sig ved mindre størrelse, mindre vægt, lavere pris og hurtigere respons tider. Konverternes gode ydeevne, samt mindre magnetiske komponenter og kapacitanser ved disse høje frekvenser, og en fortsat udvikling af halvledere, peger på at der kommer et paradigme skift inden for effektelektronik henvendt til forbrugeren inden for få år.

For at operere DC-DC konverternes halvledere ved Very High Frequency skal skifte tabene minimeres eller helt fjernes, da de ville blive alt for store. Derudover når frekvenserne øges mindskes muligheden for at benytte hard-switched gate drive, da de lider at samme tabs problemer. Lav tabs gate drive metoder kan være den eneste mulighed, specielt ved laveffekt løsninger hvor tabene i gate drivet ikke må dominere det samlede tab. Der findes forskellige resonante gate drive metoder til at overkomme tabs udfordringerne, alle med forskellig fokus såsom størrelse, pris og kompleksitet. Denne afhandling præsentere en selvoscillerende resonant gate drive metode, der kan benyttes når der som minimum er to effekttrin, metoden kan implementeres med relativt få ekstra komponenter. Det er eksperimentelt bekræftet at man kan benytte metoden både med serielt og parallelt forbundne indgange af konvertere. Sammenlignet med state-of-the-art løsninger, udmærker den beskrevne metode sig ved at have lav kompleksitet samt lave gate tab. En design metode for at benytte dette gate drive sammen med en resonant SEPIC konverter er beskrevet. Næsten alle prototyper beskrevet i denne afhandling er udviklet med billige konventionelle halvledere.

Hurtige respons tider på VHF konverter gør dem velegnet til tænd/sluk kontrol af udgangen. Tidligere implementeringer af denne kontrol metode har vidst gode resultater, men det stiller høje timing krav til alle blokkene i tilbagekoblingen. En tænd/sluk kontrol metode præsenteres der tillader brug af konventionelle integrerede chips, denne metode giver mulighed for en stabil kontrol samt høj båndbredde sammenlignet med state-of-the-art løsninger.

Mange anvendelser har ikke noget krav om galvanisk isolering. Denne afhandling beskriver en metode der skaber en DC forbindelse fra indgang til udgang af en tidligere galvanisk isoleret konverter. Denne metode består af en om konfiguration af ind og udgange, således at både udgangs effekten og effektiviteten stiger af det

samlede system, uden at der skaber yderlige stress eller ændringer i konverteren.

De opnåede resultater demonstrere at billige løsninger, baseret på silicium halvledere og ICer, kan levere god ydeevne selv med skifte frekvenser i VHF området. Halvlederne benyttet i denne afhandling har ikke været optimeret til at blive brugt ved så høje frekvenser. Med fokus på at optimering af kendte samt nye halvlederteknologier er det forventet, at VHF konvertere bliver en fast del af effektelektronikken.

Nøgleord: tænd/sluk kontrol, very high frequency, dc-dc strøm konverter, resonant konverter, switch-mode strøm forsyninger, zero-voltage switching

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Chapter 1

Introduction

1.1 Background and Motivation

Until early 2000s, and to a great extent still today as well, frequency band between 1 MHz and 30 MHz was considered a "no man's land" for magnetic materials [1]. Commonly used ferrite materials widely show significant core loss increase with frequency ($\sim f^x$, where $x > 1$), and air-core magnetic components are too big and suffer from low quality factor. In addition, electromagnetic compatibility (EMC) compliance standards pose strict requirements for conducted EMI in this frequency range. Influence of the power converter components' parasitics increases significantly as well, affecting the converter performance and requiring very good understanding of electromagnetics and fundamentals of IC processes for both coming up with good designs and debugging.

Reduction in size, weight, and cost, while maintaining high converter efficiency, is the major driver of technology advances in power electronics. We live in the time of rapid technological development, ever-increasing reliance on electronic devices and gadgets, and mobility is essential part of everyday life. In comparison, power supplies have seen steady, yet incremental improvements only, with rare game-changing leaps forward. VHF technology brings promises of significant savings in terms of physical size and weight, and eventually, cost.

To circumvent the problem of both poor magnetics performance, researchers focused on "jumping over" the 30 MHz barrier, with initial work and the most notable results from Laboratory for Electromagnetic and Electronic Systems at MIT [2–13]. Most of the work was done and published in the 2003-2014 period. Meanwhile, Electronics group in Department of Electrical Engineering, DTU, was doing research on self-oscillating class-D audio amplifiers and fast-tracking converters [14–18], and has taken interest in VHF dc-dc power conversion with first results published in 2011 [19], and subsequent research in the 2012-2014 period [20–32]. Above 30 MHz, size of energy storage components reduced significantly, with the exception of inductors - their size reduction was offset due to lack of materials for magnetic cores. Still, the ground work has been done, and highly efficient VHF power converters were

proven to be not only possible to implement, but capable of being a solid rival to conventional solutions.

1.2 Thesis Scope

The PhD thesis "Advances in Very High Frequency Power Conversion" is based on the goal to develop small, efficient, and light SMPS that operate at VHF range, while using low-cost electronic components and power semiconductor devices. The scope of this thesis is to present the research carried out for the duration of the project, from Nov 2011 to Feb 2015. Most of the scientific results of the research have been published or submitted in the form of peer reviewed conference and journal papers, as well as pending patent applications. The publications form a significant part of this thesis and are included in Appendix. The thesis supplements already published and thereby presents a more coherent and complete overview of the research work and the results obtained during the course of the PhD project.

This thesis presents advances in several key elements in dc-dc power conversion at very high frequencies: gate drivers, control, and cell stacking.

1.3 Thesis Objectives

The project aims, to great extent thanks to very recent appearance of interest in the topic, were defined qualitatively. This offered the possibility of investigation of, and advances in, several key areas of dc-dc power conversion at very high frequencies. In particular:

- A new self-oscillating resonant gate driver for class-E derived multi-cell designs is proposed, with minimum component, cost, and size requirements.
- A control method, which we term phase-shift control method, has been introduced into VHF dc-dc power conversion domain.
- Vertical cell stacking of VHF power converters.
- Topological variations of the power stages which allow direct transfer of part of the total processed power, resulting in increased power transfer and higher efficiency, while decreasing stress handling requirements of the switches.

1.4 Thesis Structure and Content

The structure and contents of the PhD thesis are visualized in the flow chart as shown in Fig. 1.1.

Chapter 1 briefly introduces the background, motivation, scope, and the objectives of the project. The overview and state-of-the-art are discussed in Chapter 2. Chapters 3, 4, and 5 discuss the particular contributions of this work to the field

of VHF dc-dc power conversion. Conclusions and author's reflections on possible continuation of the research in the future are presented in Chapter 6.

Published and submitted conference and journal papers are included in Appendices C through F as well, as illustrated in the flow chart in Fig. 1.1.

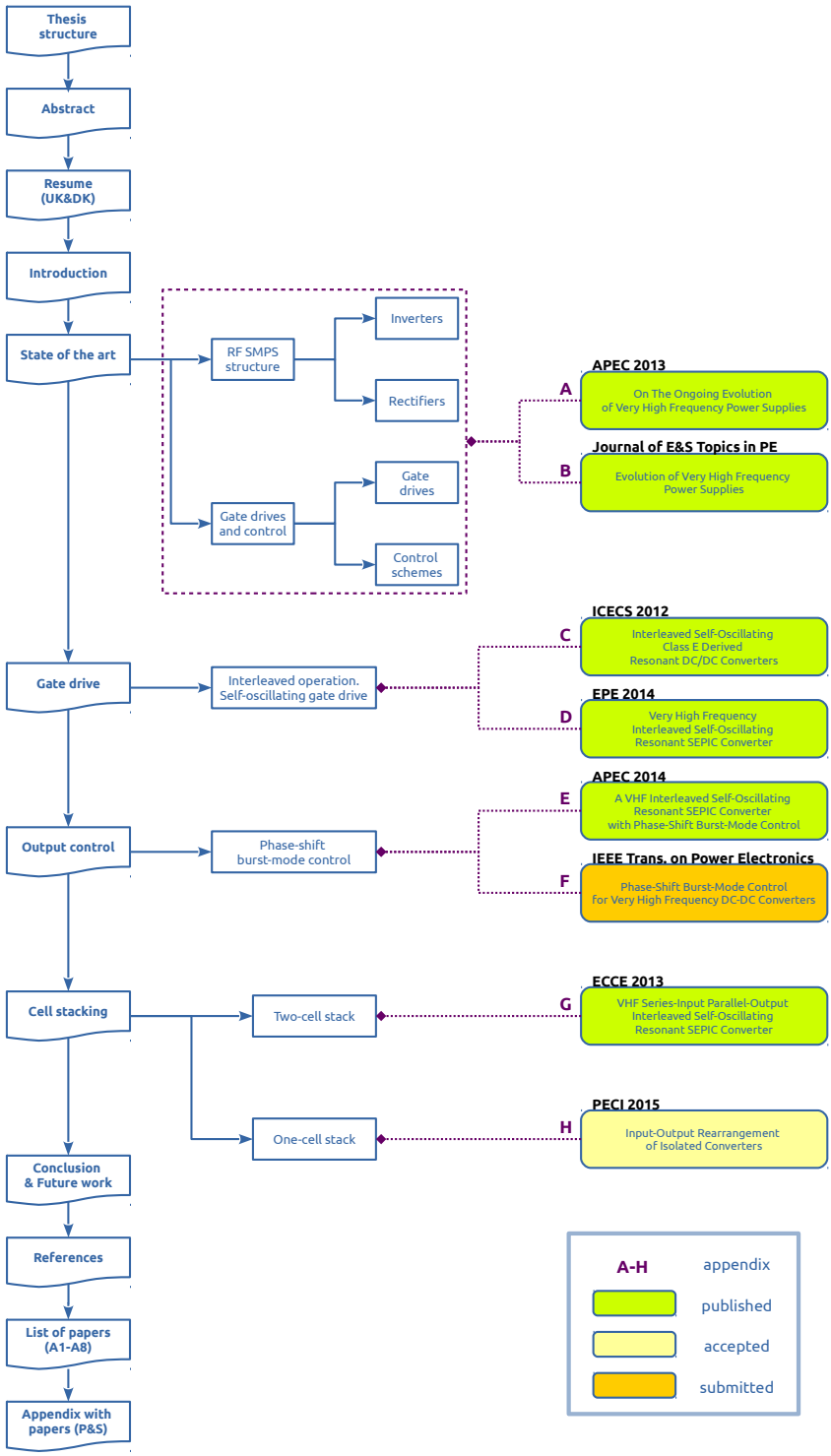

Figure 1.1: PhD thesis structure.

Chapter 2

Overview and State-of-the-Art

We realize that miniaturization and cost reduction of power supplies is desirable, and increasing operating frequency into VHF range seems to be a reasonable approach. In this chapter, an overview and state-of-the-art of VHF dc-dc converters topologies, power semiconductor gate driving methods, and output voltage/current control is presented. Advantages and disadvantages of the proposed solutions are discussed. In addition to what is presented in this chapter, more detailed information may be found in Appendices A and B.

2.1 VHF SMPS: Topologies

Fig. 2.1 shows a simplified model of a NMOS semiconductor device. If a turn-on event occurs when parasitic capacitances C_{DS} and C_{GD}, inherently present in semiconductor power devices, are charged, energy stored in these is dissipated in the device and switching loss occurs. This is a typical scenario in hard-switched converters, where the C_{DS} and C_{GD} are forcefully charged and discharged. The switching loss increases linearly with switching frequency[1], as the number of switching events increase in a given time unit, and this loss mechanism quickly reaches atrociously high levels[2].

Neglecting second-order effects, power dissipated in the semiconductor device is proportional to switching frequency, and the energy stored in its output capacitance at the moment of the switching event. Assuming that C_{DS} and C_{GD} are functions of voltage, the general expression for power loss due to their forced discharge is derived in [33]:

$$P_{sw} = f_S \int_0^V v_C \, C_{OSS}(v_C) \, \mathrm{d}v_C \tag{2.1}$$

f_S is the switching frequency, v_C is the capacitance voltage, $C_{OSS} = C_{DS} + C_{GD}$ is

[1] Switching loss increases even faster when second-order effects are included, e.g. parasitic source inductance of the switching devices, Miller effect, etc.

the small-signal voltage dependent output capacitance of the semiconductor switching device, measured at bias voltage V:

$$C_{OSS}(v_C) = \frac{i_C}{\mathrm{d}v_C \,/\, \mathrm{d}t}\bigg|_{V_C=V} \tag{2.2}$$

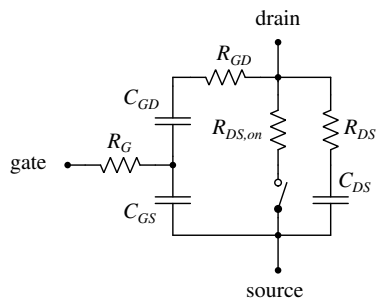

Figure 2.1: MOSFET device model.

As P_{sw} is a linear function of f_S, we realize that hypothetical loss of 1 W at 1 MHz turns into 30 W at 30 MHz. Such increase in switching loss limits obtainable operating frequency of a dc-dc converter severely. Moreover, gate loss follows the same law as well. Second-order effects induced by parasitic inductances in series with the semiconductor device terminals further reduce the upper frequency limit of obtainable switching frequency [34]. In order to design dc-dc converters with high efficiency at very high frequencies, a different approach is required.

The question arises - how do we remove the energy stored in C_{OSS} before the turn-on event? In the subsequent sections, two main approaches are discussed, and both use soft-switching to eliminate or reduce switching loss:

- dc-dc converters based on class DE, E, E/F inverters and rectifiers, and
- quasi-resonant dc-dc converters.

2.1.1 Resonant Inverters/Rectifiers

2.1.1.1 Resonant Inverters

Class E inverters have been used since late 1970s as RF power amplifiers [35]. Fig. 2.2 shows a class E inverter. Compared to class A, B, AB, C, D, and F, class E inverters have no current and voltage overlap across the main switch, which allows operation at very high frequencies. Since constructing a high-side driver at VHF is a significant challenge, the fact that there is only one low-side switch is highly beneficial as well.

To achieve zero voltage switching (ZVS), impedance of the resonant network seen from the drain node Z_{DS} needs to be inductive at the switching frequency [36]. Inductive Z_{DS} is required to allow for a resonant transition when the switching device is off. In order to obtain inductive impedance, the resonant network is tuned

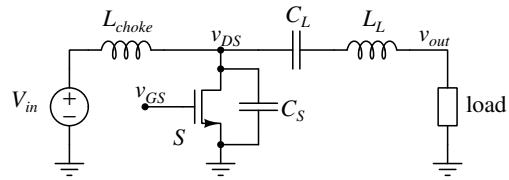

Figure 2.2: Class E inverter.

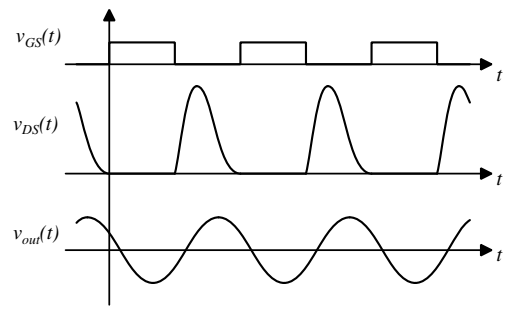

Figure 2.3: Typical waveforms of the class E inverter.

such that the resonant frequency of the C_L-L_L tank (series resonant tank, see Fig. 2.2) is lower than the switching frequency. Detailed design equations for class E inverters can be found in [19, 35–37]. L_{choke} is typically a large inductance with high impedance at the switching frequency, and it doesn't contribute to the resonant network - therefore low $\mathrm{d}i_L/\mathrm{d}t$ of the limits the system bandwidth. However, L_I may be sized down to become a resonant inductor for a minor or no penalty in efficiency, while allowing for a significantly faster transient response [10]. In addition, L_L may be reduced in size as well if C_L is turned into an ac short.

Alternative configuration of the resonant network in Fig.2.2 is proposed in [6] and shown in Fig. 2.4. This inverter requires L_I to be small and part of the resonant network, as otherwise it becomes difficult to obtain the necessary properties of the network impedance which allows for ZVS operation. In general, it is possible to obtain desired properties of the input impedance of the resonant network in Fig. 2.4 with bulk L_I, it is not recommended. Note that the load is in parallel with L_L, meaning that effective load resistance needs to be significantly higher compared to $\omega_S L_L$ to obtain the required phase of Z_{DS}. This leads to large circulating currents in the resonant tank.

A major downside of the class E inverter is high peak drain voltage v_{DS}, typically 3.6-4 times V_{in} at 50% MOSFET duty cycle [19, 36] as a function of voltage dependence of the MOSFET output capacitance, C_{OSS} [38, 39].

To alleviate the difficulty with high voltage stress on the main switch, a new inverter topology termed EF_2, or Φ_2, has been proposed in [4] and discussed in [40]. The inverter topology is shown in Fig. 2.5. The inverter operation was successfully demonstrated as a part of VHF dc-dc converters in [5, 8, 9, 41]. The topology uses a multi-resonant network to suppress second and promote third harmonic in

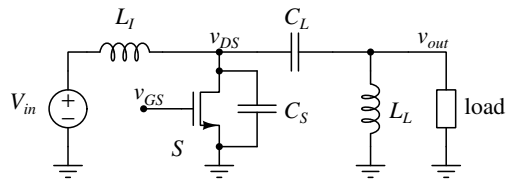

Figure 2.4: Class E inverter, alternative configuration with resonant input inductance.

v_{DS} voltage waveform. Once the desired properties of the resonant network are obtained, $V_{DS,peak}$ is reduced to ~$2 - 2.5\ V_{in}$.

A converter using class-EF_2 inverter topology is penalized by extra circulating second harmonic current in $C_2 - L_2$ leg and extra space requirements. The gains of using a MOSFET with 30% lower breakdown voltage usually compensates for the extra loss in the second harmonic leg. In addition, the complexity is lower compared to two power stage cells sharing the input voltage. The subject of converter stacking is discussed in more detail in Chapter 5.

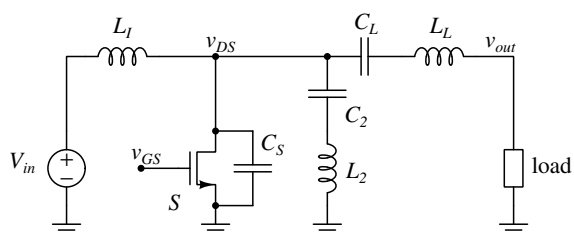

Figure 2.5: Class EF_2 inverter.

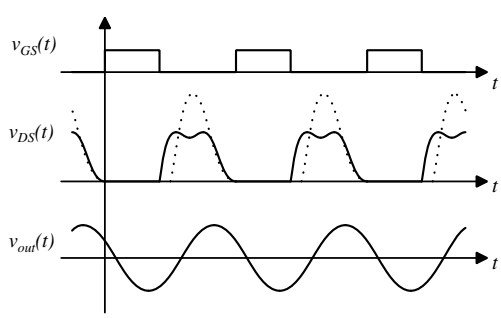

Figure 2.6: Typical waveforms of the class EF_2 inverter.

Another approach to addresses excessive voltage stress is the use of a half-bridge inverter, with an appropriate resonant tank to ensure ZVS operation. Fig. 2.7 and 2.8 shows the class-DE and LLC inverters, respectively. A VHF class DE inverter has been demonstrated in [26] only. In half-bridge inverters the voltage stresses on the main switches equal V_{in}.

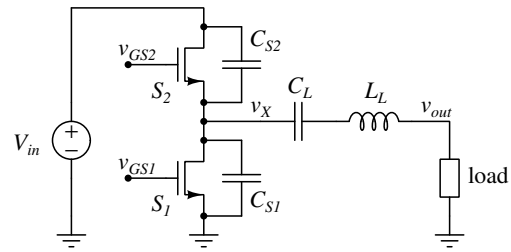

Figure 2.7: Class DE inverter.

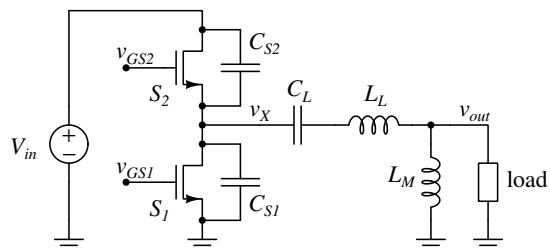

Figure 2.8: LLC inverter.

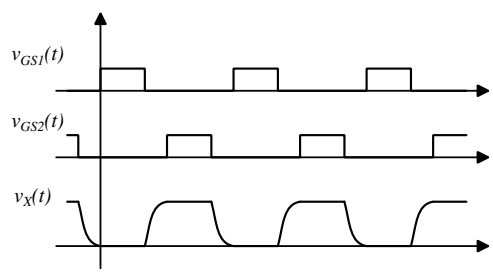

Figure 2.9: Typical waveforms of a half-bridge resonant inverter.

The greatest challenge with half-bridge based inverters is the necessity for a high-side switch, and therefore a high-side gate driver[2]. The difficulty lies in lack of off-the-shelf gate drivers with propagation delays in the order of few nanoseconds with fast rising and falling edges. It is however expected that advances in power semiconductors (both with Si and GaN technologies) and integrated circuits are going to make this option more and more appealing. The limitation is not inherent to physics of silicon IC processes, but in the lack of demand on the market.

Drain waveforms in single-ended topologies (topologies with only a single switch in their inverter part) discussed so far depend on nonlinearity of the MOSFET output capacitance C_{OSS}. C_{OSS} is low at high v_{DS} and high at low v_{DS}. As a result, the converter peak voltage is higher than predicted by linear capacitance. Half-bridge topologies do not suffer from this effect significantly, because the equivalent capacitance seen by v_X node is symmetrical around $V_{in}/2$.

An illustration of semiconductor voltage stress is shown in Fig. 2.10. For high input voltages (e.g. in offline converters) it is extremely valuable to implement anything but a class E inverter operated at 50% modulation cycle, not only because it is nearly impossible to find an appropriate switching device, but also for extra spacing (8 mm according to IPC-9592B standard, 7.5 mm for uncoated and 3.85 mm for coated conductors in every direction according to IPC-2221A) from the switching node. In general, a choice of the inverter topology depends heavily on specifications. In several papers VHF converters have been implemented using laterally diffused (LD) RF MOSFETs, with peak voltages of above 400 V [5]. These devices are extremely expensive, however the reason is significantly over-sized die area [8] for heat absorption/sinking (due to class A or AB operation) and high margin necessary due to low production quantity. Peak voltages below 200 V allow the use of trench MOSFETs. To author's best knowledge, super-junction (SJ) technology has not proved to be a viable solution for high voltage converters. It is expected that MOSFETs based on gallium-nitride technology will eventually dominate the VHF dc-dc power conversion regardless of the input voltage, but will make its entrance into the market at higher voltages.

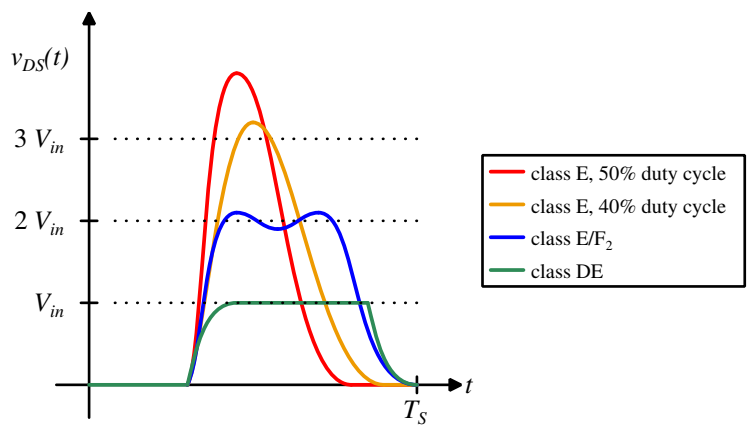

Figure 2.10: Peak MOSFET voltage stress comparison for class E, EF$_2$, and DE inverter topologies.

2.1.1.2 Resonant Rectifiers

Typical resonant rectifier topologies used in VHF converters are in fact the same topologies presented in Section 2.1.1.1. They are however easier to implement since the operation does not necessarily require controllable switches. Most commonly used rectifiers so far are class-E low dv/dt [42], low di/dt [43], and class-DE (half-wave) [44]. These rectifiers are shown in Fig. 2.11, Fig. 2.12, and Fig. 2.13, respectively.

Synchronous rectification is possible with the use of controllable switches, and MOSFETs are good candidates since they already have inherent body diodes. However, for a significant improvement in overall efficiency precise timings need to be gen-

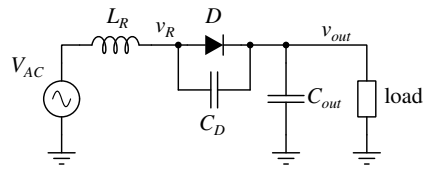

Figure 2.11: Class E low dv/dt rectifier.

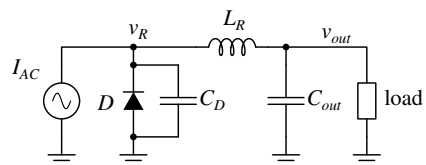

Figure 2.12: Class E low di/dt rectifier.

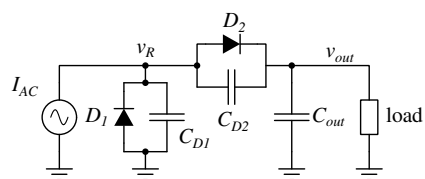

Figure 2.13: Class DE half-wave rectifier.

erated, as performance of the MOSFET body diodes is usually far from desirable. When the gating loss and extra space for the gate drivers are introduced into the equation (resonant or otherwise), it may still be only a small improvement compared to a solution with diodes only. With development of GaN semiconductors and their ever-increasing yield and performance, both gate and conduction loss will be reduced significantly compared to the silicon-based solutions.

2.1.2 Quasi-Resonant Converters

As opposed to fully resonant power converters discussed in Section 2.1.1, quasi-resonant converters do not have resonant tanks per se, and do not generate sinusoidal waveforms. Rather, resonant voltage and current transitions occur between neighboring switching events of two different devices (dead time). These converters typically have fewer components compared to their fully resonant counterparts [45], and in certain cases they are more flexible if operated under variable frequency control [46].

However, the downside is that they can obtain ZVS operation only for a small range of output voltages. In case of the QR buck converter the ZVS voltage range is $V_{in}/2 < V_{out} < V_{in}$, while for QR boost ZVS occurs for $V_{in} < V_{out} < 2\ V_{in}$. The range is further limited by nonlinearity profile of the capacitance seen from the switching node. This is the major limitation of the quasi-resonant converters, but it can be addressed with the use of synchronous rectification. By extending

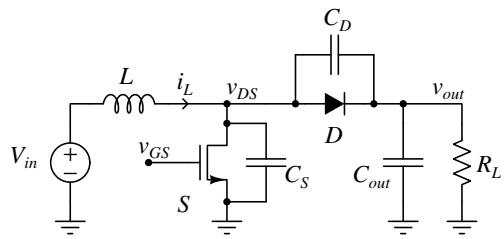

Figure 2.14: Quasi-resonant boost dc-dc converter.

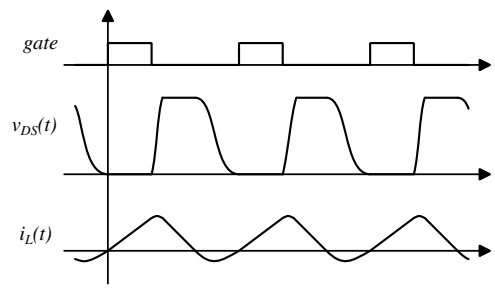

Figure 2.15: Quasi-resonant converter waveforms.

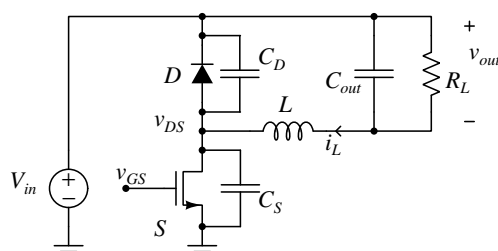

Figure 2.16: Quasi-resonant buck dc-dc converter with a low-side switch and non-grounded load.

the on time of the second switch, it is possible to provide additional energy for the resonant transition to obtain ZVS. Due to their simplicity, it is expected that their use in low-end VHF frequency domain to increase significantly in the near future.

2.2 Control Schemes

Even though VHF dc-dc power conversion gained interest only recently, several control methods have been proposed, with varying success in output voltage control and EMI performance: on/off (burst-mode), cycle-skipping (thinned-out), and frequency modulation.

2.2.1 On/Off Control

Essentially a family of control methods, on/off control is the most versatile, as it demonstrates consistent performance parameters under wide load range conditions. Assuming tightly regulated output voltage, the converter can be modeled as an input voltage dependent current source, $I_0(V_{in})$. The converter needs to be designed such that it is capable of delivering (at least) 100% load current at the minimum V_{in}. Output capacitance is chosen to provide required ripple at the modulation frequency (usually highest at 50% load).

2.2.1.1 Pulse Width Modulation at Constant Frequency

This is probably the most straight-forward control method from a classical power electronics engineer's point of view. The converter is modeled as a current source which produces current pulses at the switching frequency according to the control signal determined by the controller $G(s)$. The plant and the controller are described by linear models, and all the design practices from conventional power converter control design apply. It also means that PWM method suffers from the same issue: transient response is slow and may exceed the steady state ripple by orders of magnitude. Since transient response of the power stage is extremely fast (typically several switching cycles) and the low frequency transfer function has only a single pole, alternative control methods have been investigated.

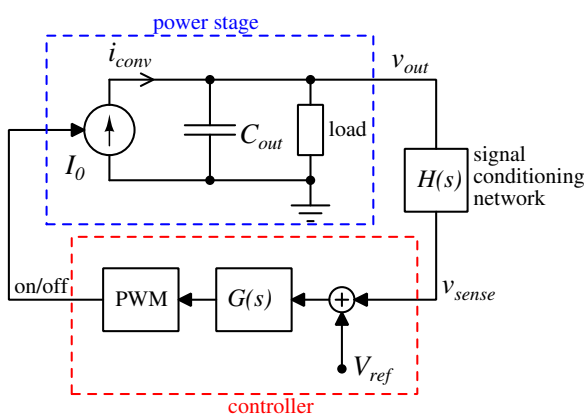

Figure 2.17: Low frequency model of a VHF converter with PWM control.

2.2.1.2 Hysteretic Control

Hysteretic control method belongs to a group of methods known as self-oscillating or "sliding-mode" control[14, 47].

Fig. 2.19 and Fig. 2.20 show the low frequency model of a converter operated with hysteretic control and typical waveforms. A comparator with a hysteresis is used to set upper and lower bounds on the output voltage. Theoretically, modulation

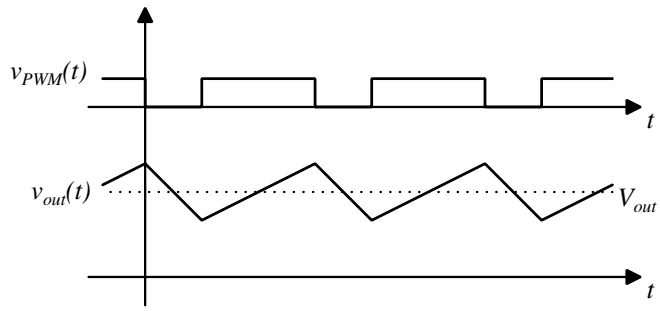

Figure 2.18: Typical waveforms of a VHF converter with PWM control.

frequency changes from 0 at (0% and 100% load) to $f_{M,max}$ (at 50% load). In practice, the converter may be overdesigned for around 10-20% of output power to limit the modulation frequency at heavy load and to provide headroom for component tolerances. At low load the frequency is limited by the control circuit power consumption and/or minimum load. Since the output voltage does not leave the preset voltage window, the technique provides exceptional performance in terms of transient response. However, very low propagation delay, compared to a modulation period, is allowed (as close to zero as possible). This severely limits the choice of the comparator and the gate driver design.

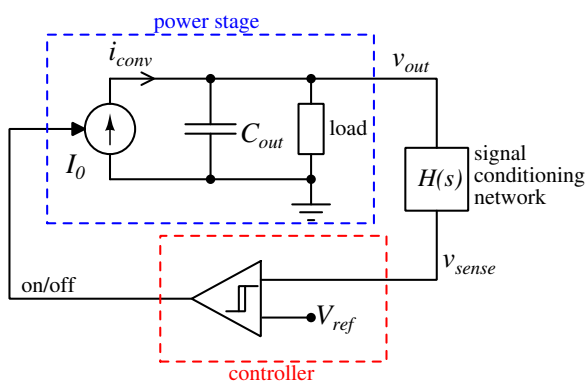

Figure 2.19: Low frequency model of a VHF converter with hysteretic control.

2.2.2 Cycle-Skipping Control

If we consider class E rectifier from Fig. 2.12, it is possible to add a controlled switching device S_D in parallel to the diode D. If S_D is turned on only when the diode is supposed to be on, synchronous rectification is obtained. If S_D is kept on for one whole period, no power is delivered to the load from the input side. By sending the turn-on pulses in a controlled and predictable manner, output voltage control can be achieved [48, 49].

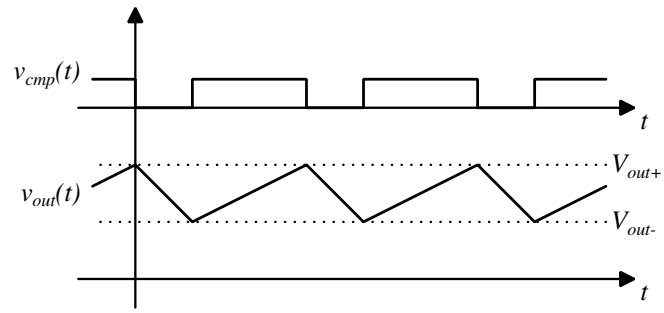

Figure 2.20: Typical waveforms of a VHF converter with hysteretic control.

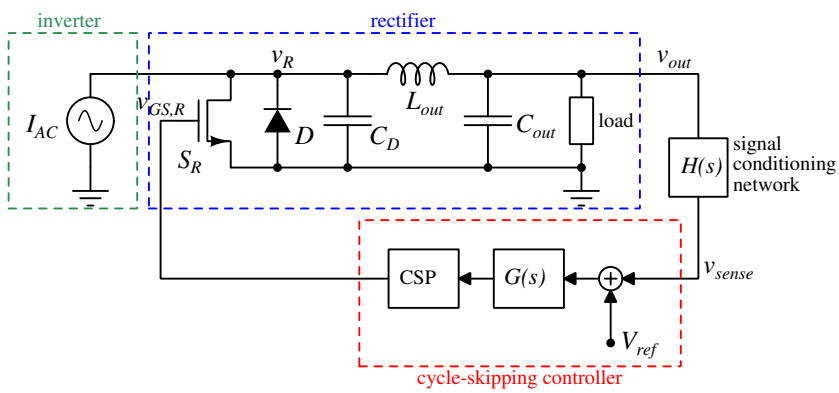

Figure 2.21: VHF converter with cycle-skipping control.

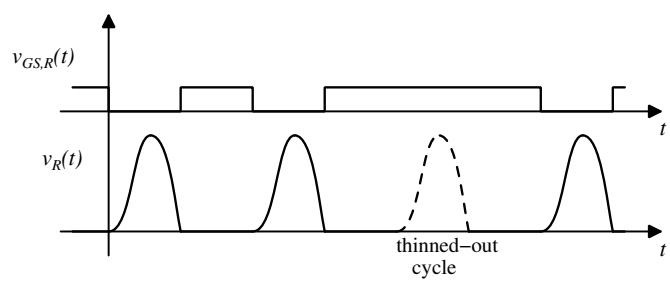

Figure 2.22: Typical waveforms of a VHF converter with cycle-skipping control.

Cycle-skipping (thinned-out) method is best suited for applications where fine regulation around full load is required (e.g., battery charging, non-dimmable LED lighting), as under light load conditions efficiency would suffer a great penalty due to large circulating currents in the resonant tank with no power delivered. In addition, volt-second balance on L_{out} will cause the peak voltage on the D-S_R pair to increase when the cycles are skipped [49]. Therefore, the MOSFET/diode pair in the rectifier need to be sized to significantly higher voltage stress.

The major benefit is smaller output filter and low EMI in comparison with burst-mode control - it affects the output on "several cycles at a time" basis (2-16), which causes much smaller perturbations at the input side. It is within reason to assume the method is similar to PWM burst-mode control at significantly higher frequencies.

2.2.3 Frequency Modulation Control

Frequency modulation control is attractive because it allows the converter to "adjust" its resonant network impedance on-the-fly, depending on its input/output voltage or load, thus running continuously and generating less EMI compared to burst-mode control schemes.

However, the method typically cannot cover 0% to 100% load variation range. Moreover, a wide frequency band is often required to provide the desired impedance change. There is also a trade-off between the frequency range and the amount of circulating currents, which implies efficiency penalty. It is therefore a common practice to combine this method with some kind of on/off control.

In general, it is not possible to use this method together with multi-resonant converters as their performance drastically depends on the input impedance properties of the resonant tank. Regarding the topologies discussed in Section 2.1, all except for class EF_2 inverter can use this control scheme, as long as the duty cycles of the controlled switches are adjusted as the frequency changes[2].

2.3 Gate Drives

2.3.1 Hard Switching Gate Drives

Even though hard-switching gate drives are considered too lossy for VHF operation, they are still the most versatile and space-saving compared to most other options as long as the heat produced by power dissipation in the gate driver is manageable. Power dissipated due to hard-gating, assuming linear gate capacitance C_{ISS} is:

$$P_{gate,HS} = f_S \, C_{ISS} \, V_{GS}^2 \tag{2.3}$$

Note that (2.3) is independent on gate resistance. Hard gating is naturally more interesting at the lower end of frequency range (around 30 MHz) and high power levels (tens to hundreds of watts), as the gate loss diminishes percentage-wise in the overall power loss budget. Since the gating loss is proportional to V_{GS}^2 and C_{ISS}, it is more important to reduce the switch threshold and gate voltage at which the MOSFET achieves full turn-on than it is to reduce C_{ISS} from the power loss perspective. Since C_{ISS} and gate resistance R_G form a first-order low pass filter and thus soften the transition edges, it is necessary to reduce either or both C_{ISS} and R_G.

[2]Time necessary for resonant transitions to complete depends on voltage and current initial conditions in the resonant elements, and therefore is an indirect function of switching frequency.

As the semiconductor devices improve, especially with the use of GaN technology, it is expected that this type of gating will dominate the VHF dc-dc conversion. During the major part of this project, the semiconductor devices with characteristics which allow hard gating were either unavailable or extremely expensive. At the time of writing the dissertation, commercial and prototype parts with extremely low $C_{ISS}\,R_{DSon}$ product are becoming available.

2.3.2 Resonant Gate Drives

To suppress gating loss and recycle the energy used for charging and discharging the gate capacitance, resonant gate drives have been introduced. In [4–6, 9] fixed frequency gate driver implementations have been proposed, based on VHF inverters. Fig. 2.23 shows one such implementation using a second harmonic class E inverter. An advantage of this implementation is a half-sine waveform, which produces lower gate loss compared to the full-sine waveform[3]. Assuming that gate resistance R_G is small compared to impedance of C_{ISS} at switching frequency, gating loss of a full-wave resonant gate driver is given as:

$$P_{gate,FW} = R_G\, i_G^2 = R_G \left[2\,\pi\, f_S\, C_{ISS}\, V_{GS}\right]^2 \tag{2.4}$$

where i_G is the gate current. A half-wave resonant gate driver generates close to half as much assuming that V_{GS} is the same, depending on the actual resonant frequency in the driver:

$$P_{gate,HW} = \frac{1}{2\,\alpha}\, R_G \left[2\,\pi\,\alpha\, f_S\, C_{ISS}\, V_{GS}\right]^2 \tag{2.5}$$

where α is the ratio between the switching frequency and the equivalent resonant frequency of the gate driver. Note that $P_{gate,HW}(\alpha = 1) = 0.5\, P_{gate,FW}$, which is the case when the half-sine waveform has exactly the same frequency as the full-sine. In [45] a fixed-frequency oscillator with gate bias voltage modulation has been proposed (see Fig. 2.24), and demonstrated in a quasi-resonant boost converter. VCO produces a sinusoidal voltage waveform, while the bias voltage shifts the waveform up and down, thus changing the duty cycle. However, the converter is operated better if the frequency is adjusted at the same time as the duty cycle. The downside of these techniques is the complexity, significant space on a PCB, and extra loss due to all the additional elements.

2.3.3 Self-Oscillating Gate Drives

If a feedback is taken from the resonant inverter output and fed back to the MOSFET gate via a resonant network, a self-oscillating power stage is obtained. The transfer function from the MOSFET drain to gate needs to have desired amplitude and phase characteristics to obtain the proper operation. Theoretical and experimental work using this idea on a class E inverter is provided in [50] and shown in Fig.

[3] Weather sum of gate driver loss and gate loss is going to be lower for the half-sine gate driver is implementation-specific.

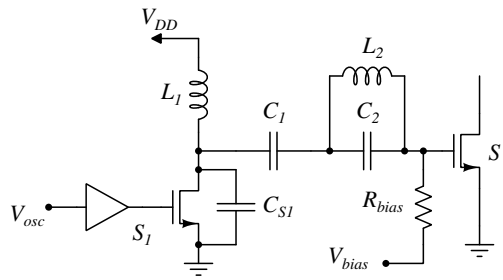

Figure 2.23: Second harmonic class E gate drive. Gate bias voltage is set to a constant value.

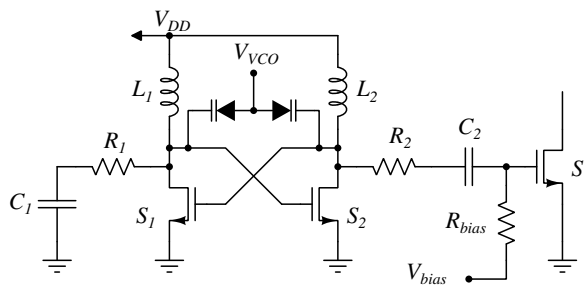

Figure 2.24: Voltage controlled oscillator with gate bias voltage modulation. Impedances seen from both outputs of the oscillator are matched.

2.25. In [19] the idea has been extended on a dc-dc converter composed of a class E inverter and class E rectifier. In [30, 32] another approach using parasitic coupling through C_{GD} was proposed, and demonstrated on resonant SEPIC converter and class DE inverter with a class E rectifier. The technique allows adjustment of both the switching frequency and the duty cycle to obtain output voltage control by varying gate bias voltage only.

Both of these techniques require an extra inductor per inverter switch in the feedback path, which takes extra space on the board. Another challenge with the resonant gate driver is linear dependence of the gate voltage amplitude on the input voltage, and additional steps need to be taken to ensure proper operation over the input voltage range.

2.3.4 Conclusion

Fig. 2.26 demonstrates gate loss of the hard-switched and resonant gate drives vs. frequency of a MOSFET with $C_{ISS} = 100$ pF and $R_G = 1\ \Omega$, according to (2.3), (2.4), and (2.5). The following assumptions are made:

- hard-gating: v_{GS} ranges from 0 and V_{GS} and voltage transitions occur instantly

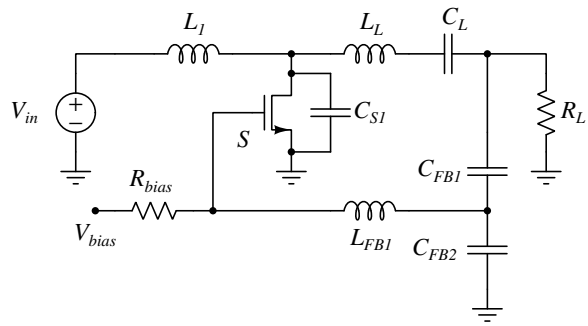

Figure 2.25: Class E oscillator.

- full-wave resonant gating: v_{GS} is a sinusoidal waveform with amplitude V_{GS} and no offset
- half-wave resonant gating: v_{GS} is a half-sine waveform that ranges from 0 to V_{GS}
- R_G C_{ISS} time constant is small enough that it doesn't introduce significant distortion in v_{GS} waveform.

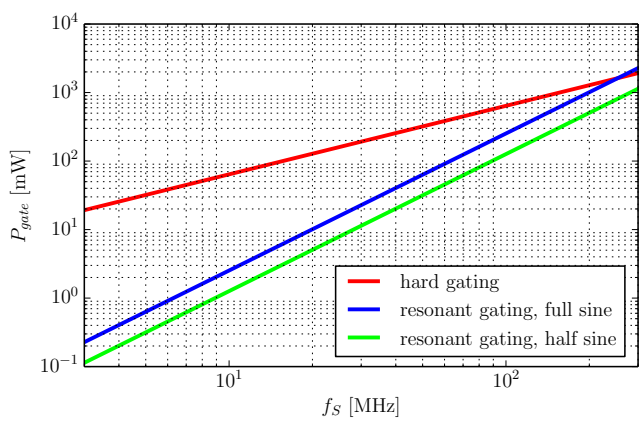

Figure 2.26: Gate loss of a MOSFET device with $C_{ISS} = 100$ pF and $R_G = 1\ \Omega$ vs. frequency.

For this particular case, resonant gating techniques have a significant lead up until around 200 MHz. If the resistance was 10 times lower, the gate loss for resonant gating would reduce by a factor of 100, pushing the crossing point with hard gating loss curve to above 20 GHz (!). This illustrates importance of keeping R_G as low as possible for the resonant gating. Optimization of the gate interface for very low R_G keeps the gate loss low and the resonant solution ahead, since such optimization does not affect hard gating. Reducing C_{ISS} is beneficial for hard gating, but even

more so for the resonant drivers as the circulating currents are proportional to $C_{ISS}{}^2$. Above 200 MHz the difference vanishes for the first two techniques, but the loss is already close to 2 W in the gate only, strongly suggesting that a different switching device is necessary. On the other hand, at 30 MHz the gate losses in the resonant drivers are an order of magnitude smaller.

This brief analysis does not include the loss in the gate driver itself. For the hard-gating driver, loss can easily be up to 20% of the gate loss (depending on the implementation), while in the case of the resonant gate drive methods the percentage can be even higher. Passive solutions have the advantage due to typically high Q factors of inductors and capacitors.

The most important conclusion is that if we want to increase the frequency and keep the gate loss as low as possible, we should go for a resonant gate driver

2.4 Summary

In this chapter, advantages and disadvantages of most common VHF converter topologies, control methods, and gate drive schemes have been discussed. State-of-the-art solutions are described for the critical problems in VHF dc-dc conversion, which forms the basis for advances proposed in the following chapters. In particular, Chapter 3 shows a self-oscillating gate-drive scheme. A burst-mode control method is proposed in Chapter 4. Cell-stacking configurations are discussed in Chapter 5.

Chapter 3

Interleaved Self-Oscillating Resonant (ISOR) Gate Drive

Non-resonant gate drive is acceptable when the power loss incurred is a small portion of total processed power. Resonant gate drive methods described in Section 2.3 add complexity, require significant amount of space, or both. In this chapter, a new gate drive method with minimal space and cost requirements is proposed, suitable for operation of at least two resonant power stages (two-cell design).

3.1 Principle of Operation

Fig. 3.1 shows the proposed network in its original form:

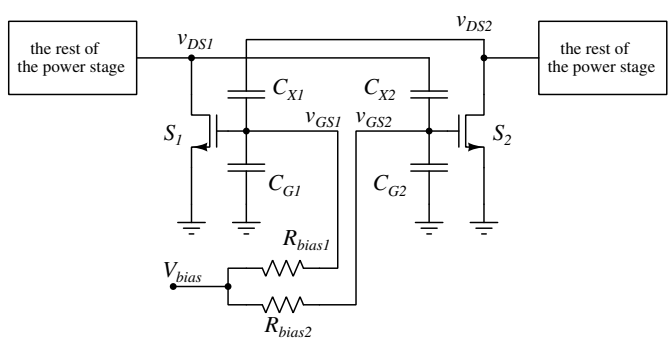

Figure 3.1: Interleaved self-oscillating resonant (ISOR) gate drive.

The capacitor pair C_{X1} - C_{G1} forms a voltage divider from the drain-source port of S_2 to the gate-source port of S_1. DC components of v_{GS1} and v_{GS2} is set by voltage source V_{bias} via resistors R_{bias1} and R_{bias2}. In the same manner, the capacitor pair C_{X2} - C_{G2} forms a voltage divider from the drain-source port of S_1 to the gate-source port of S_2:

$$v_{GS1}(t) = \frac{C_{X1}}{C_{X1} + C_{G1}} v_{DS2,AC}(t) + V_{bias} \tag{3.1a}$$

$$v_{GS2}(t) = \frac{C_{X2}}{C_{X2} + C_{G2}} v_{DS1,AC}(t) + V_{bias} \tag{3.1b}$$

At very high frequencies, capacitances C_{12} and C_{22} may be completely composed of $C_{ISS} = C_{GS} + C_{GD}$, and the only added components are C_{11} and C_{21}. This is an easy substitution given that C_{ISS} is usually a weak function of v_{DS}. Fig. 3.2 shows the respective drain and gate waveforms.

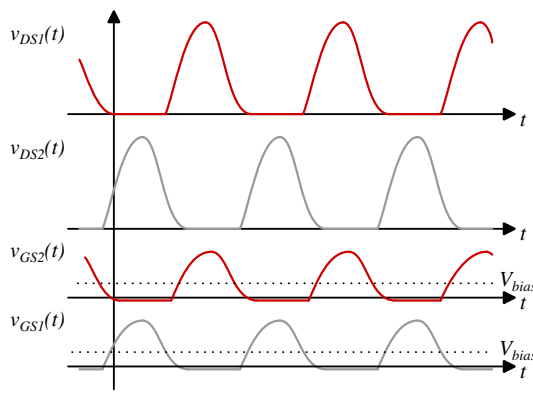

Figure 3.2: Voltage waveforms of a class E inverter with ISOR gate drive.

The added components introduce insignificant loss into the converter (see Appendix F). The coupling capacitors are with very high Q, e.g. 4.7 pF ceramic NP0 capacitors from GJM series by Murata has Q > 1000 below 300 MHz [51]. The biasing resistors are in 500 Ω - 1 kΩ range and driven by gate voltage only.

3.2 Design Considerations

- Cross-coupling loops need to be electrically small in order to minimize ringing in the gate driver network. If that is not possible (e.g. parasitic inductance of device package leads), damping resistors in series with C_X capacitors could be used to lower the Q of potential high frequency resonances within the gate drive network.
- Small difference between v_{GS1} and v_{GS2} is desirable during the converter startup, as it shortens the turn-on transient. To achieve that, the biasing resistors R_{bias1} and R_{bias2}, may differ by 10-20%, providing different time constants with the gate capacitances. The difference between R_{bias1} and R_{bias2} should be chosen such that they don't affect the gate waveform significantly when the converter is running.
- Charge injection from the drain node of the same MOSFET via C_{GD} reduces the amplitude of v_{GS}. Usually this is not a significant problem at low input

voltages, where $C_X \gg C_{GD}$. But as the input voltage is higher, C_X is reduced for the same gate voltage swing. Therefore, it may become necessary to add external capacitance in parallel to C_{GS}, which in turn allows increase in C_X. Fig. 3.3 shows the coupling with detailed gate terminal.

- Class-E derived resonant inverters, with a notable exception of the resonant SEPIC converter (Fig. 3.4) require phase-shift between the drain and the gate voltage greater than 180° [19]. The capacitive cross-coupling network provides the shift of 180° only, implying that a additional delay needs to be provided. The easiest way to do that is adding a resistor in the feedback path, in series with C_X capacitors.

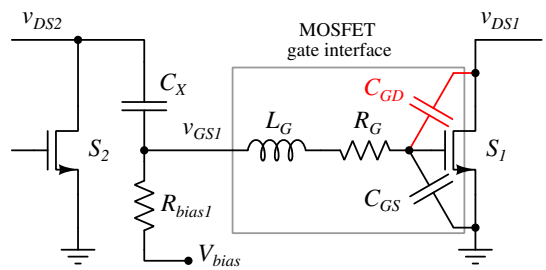

Figure 3.3: Part of the resonant gate drive network with included parasitics.

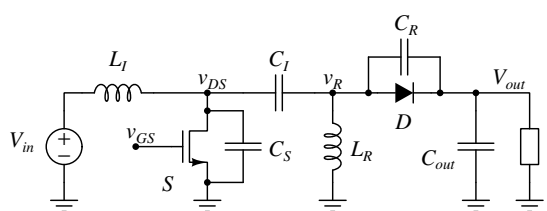

Figure 3.4: Resonant SEPIC dc-dc converter.

3.3 Experimental Results

ISOR gate drive was first tested on a 110 MHz resonant boost converter (Appendix C, see Fig. 3.5), using a high-end 65 V LDMOS device with very low parasitics, achieving peak efficiency of 89%. In addition, several resonant SEPIC prototypes (Appendices D, G, E, F, see Fig. 3.6) with operating frequencies in the range of 33-49 MHz and efficiencies from 82% to 87%.

High efficiency and waveform symmetry was achieved in all cases without significant effort, and no additional tuning of the converter particular power stages was necessary. Note that the converter layout was highly symmetric in each case, in order to assure that the converter parasitics are balanced. Still, mismatch between the parasitics would be easily determined with the use of an impedance analyzer.

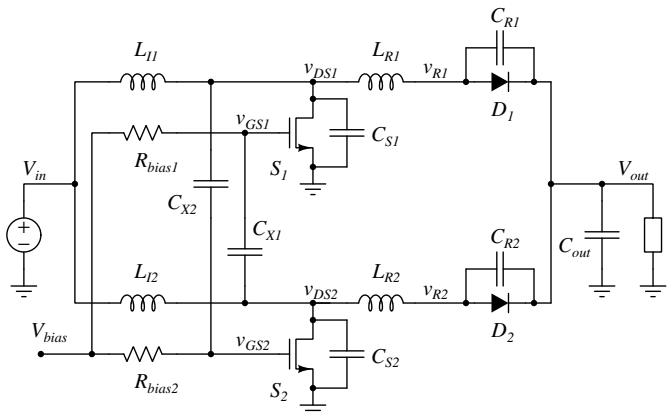

Figure 3.5: ISOR boost power stage.

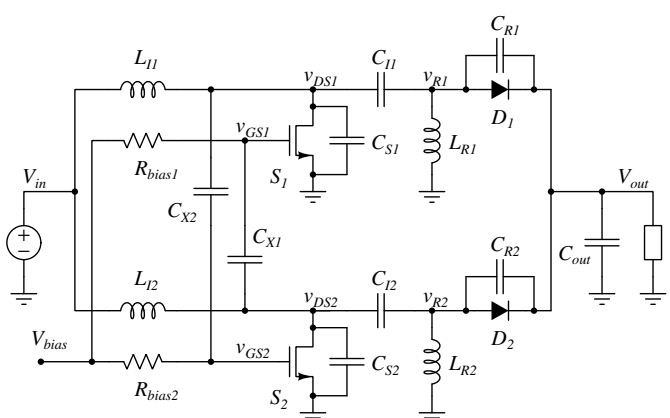

Figure 3.6: ISOR SEPIC power stage.

Chapter 4

Phase-Shift Burst-Mode Control

As we have seen in 2.2, burst-mode control is so far the most common technique of output voltage/current control in VHF dc-dc converters. PWM burst-mode control provides constant modulation frequency, but has relatively poor dynamic performance in comparison with hysteretic control. On the other hand, to operate properly, implementations of hysteretic control dictate very strict requirements for total delay in the feedback loop compared to the modulation period, thus limiting the choice of gate driver and ICs. In this section the phase-shift control method is described, which achieves very similar dynamic performance as hysteretic control, but has significantly lower constraints on time delay throughout the feedback loop. Similar to hysteretic control, phase-shift control is also self-oscillating (sliding-mode) control.

4.1 Principle of Operation

Phase-shift control is easiest to understand by comparing it to hysteretic control (see Fig. 4.1). Let us assume 50% modulation cycle and the modulation period $T_M = 1/f_M$. Output voltage v_{out} ranges from $V_{out} - V_H/2$ to $V_{out} + V_H/2$, which is set by the hysteretic comparator. Assuming that the converter behaves like a constant current source and an ideal output capacitive filter C_{out}, V_{out} lies in the middle of the output voltage window. It takes $T_M/4$ for v_{out} to increase from V_{out} to $V_{out} + V_H/2$. Reaction time in the feedback loop is ideally zero.

To maintain the same behavior of v_{out}, voltage domain hysteresis can be translated into time domain, by setting a single threshold voltage at V_{out} and increasing the reaction time to $T_M/4$. This transformation preserves the voltage waveform, but significantly relaxes requirements for the propagation delay through the feedback loop. Moreover, the transformation allows the use of gate drivers with slow start and IC circuits with high propagation delays, while keeping up most of the performance benefits of the hysteretic control method.

As there is no such thing as "free lunch" - where is the downside of this trade off?

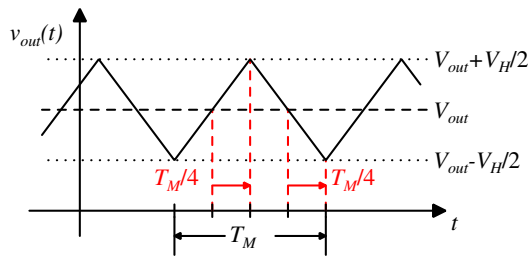

Figure 4.1: Transformation from hysteretic to phase-shift control. Note the equivalence of voltage and time windows.

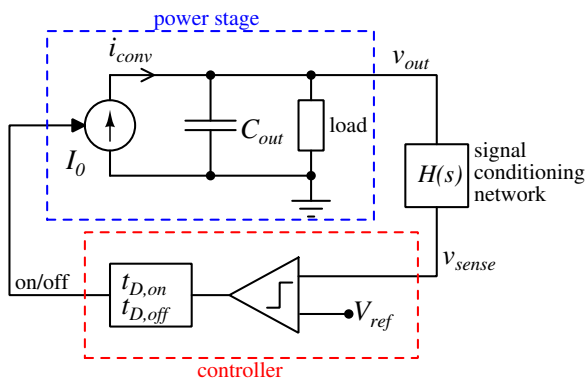

Figure 4.2: Low frequency model of a VHF converter model with phase-shift control.

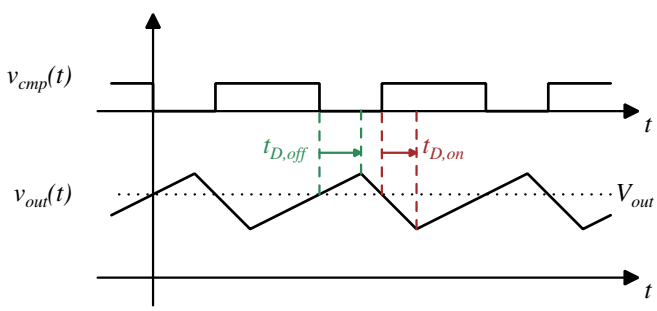

Figure 4.3: Voltage waveforms of phase-shift control.

Since the excursions of the output voltage ripple are defined in time rather than in voltage domain, the average of v_{out} becomes a function of load. The dependence can be made such that is not significant for a given application, but has been observed in both Appendix E and Appendix F. The said issue is relatively easy to compensate for, either by feeding the comparator output v_{cmp} back to the sense or the reference node, or by addition of a PI compensator for the comparator reference.

4.2 Design Considerations

The analysis above assumes a feedback loop with:

- symmetrical propagation delay. Weather this condition is fulfilled is highly implementation specific, and depends on choice of the comparator and the gate driver propagation delays.
- slope-independent propagation delay. In real comparators, propagation delay is usually dependent on $\mathrm{d}v/\mathrm{d}t$ at its input. This will cause difference from predicted v_{out} and f_M dependence on the load. Dependence of v_{out} will decrease, and f_M range will increase.
- no voltage domain hysteresis. Most comparators have in-built hysteresis of usually a few mV. The hysteresis increase noise immunity and decreases f_M in applications where very low output ripple is required.
- arbitrary delay placement. Ideally it doesn't matter where the delay comes from. However, if an analog low-pass filter with significant delay is a part of $H(s)$, the signal at the input of the comparator is attenuated. This is likely to cause instability in f_M or, if the rest of the circuit is fast and sensitive, f_M may become only an order of magnitude lower than f_S. The designer is therefore encouraged to implement the delay in the comparator and the gate driver.

4.3 Experimental Results

Appendices E and F show theoretical and experimental work on phase-shift control on ISOR SEPIC converters (see Fig. 3.6) with two different comparators and sensing networks (Fig. 4.4).

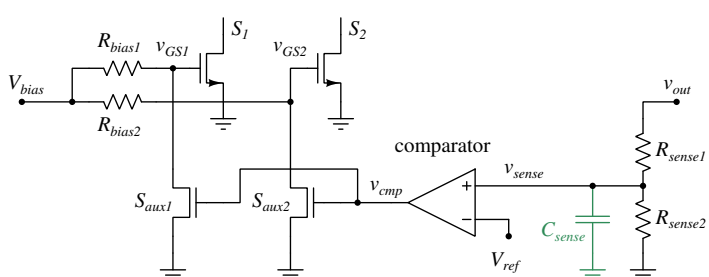

Figure 4.4: Implementation of the phase-shift controller.
Appendix E: AD8468 comparator (t_D =45 ns) with C_{sense}.
Appendix F: NCX2200 comparator (t_D = 800 ns) without C_{sense}.

Appendix E presents an implementation which operates at close to 300 kHz of modulation frequency f_M at 50% load, using AD8468 comparator with propagation delay of $t_D = 45$ ns. This is among highest (to the author's best knowledge, the highest) burst-mode modulation frequency in VHF converters published thus far.

Since $t_D \ll T_S/4$ (significant delay was introduced by the low-pass noise filter in the sensing network), this implementation could have easily achieved even higher modulation frequency.

Implementation with NCX2200 comparator with 800 ns of typical propagation delay is shown in Appendix F, with $f_M = 143$ kHz at 50% load. In this work, the major part of the loop propagation delay is provided by the comparator. The sensing network is a resistive voltage divider only, meaning the comparator is responsible for almost twice the typical propagation delay, due to in-built hysteresis t_D dependence on input voltage $\mathrm{d}v/\mathrm{d}t$. In addition, a comparison was made with state-of-the-art hysteretic controllers in terms of voltage control capability

These results show that the control method is capable of matching hysteretic control in most aspects of its performance for a significant gain in comparator and gate driver design flexibility, together with potential cost reduction.

Chapter 5

Cell Stacking

In power electronics, it is often of interest to obtain large voltage transformation ratio $M = V_{out}/V_{in}$. This is particularly of interest for offline applications, power supplies for PCs, etc. Due to their typically high requirements for semiconductors voltage handling, using a single VHF converter off a 400 V bus at the time of writing the thesis pose a nearly impossible engineering problem. A configuration with multiple cells where inputs are connected in series and outputs in parallel (SIPO) is therefore useful for addressing this challenge, in the sense that it makes the challenge manageable.

5.1 Two-Cell Stack

Let us consider the following scenario: a single-cell converter with voltage transformation ratio of $M = 0.5$, input voltage V_{in}, output voltage V_{out}, and the DC component of the input current I_{in}. Assuming class-E type inverter operated at 40%, $V_{DS,peak}$ of around $3 - 3.5\,V_{in}$ is expected. If two isolated converters are connected in series at their inputs hoping that their average input DC currents are the same, $I_{in1} = I_{in2} = I_{in}$ (a condition necessary to preserve charge balance on C_{in1} and C_{in2}), and their input voltages are the same, $V_{in1} = V_{in2} = V_{in}/2$, their peak drain voltages are the same as well, $V_{DS1,peak} = V_{DS2,peak} = 1.5\,V_{in}$, which is a significant improvement over the original case. Fig. 5.1 shows a two-cell SIPO stack configuration.

Assuming all the switching devices in the inverter side are the same, the minimum number of cells N_{min} is the smallest integer for which $V_{DS,peak} < BV$ (semiconductor device's breakdown voltage). What is the optimal number of cells N_{opt}? Input impedance of the stacked converters needs to be half the size compared to that of the single-cell converter. For the input inductors this is usually unfavorable since, for a fixed diameter, resistance drops linearly with reduction of length, but inductance drops at a faster than linear rate[1] [52, 53]. Current flowing through the MOSFETs

[1] Depending on the diameter to length ratio.

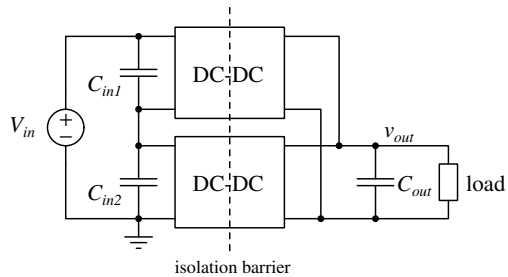

Figure 5.1: VHF dc-dc converters: two-cell stack with inputs in series and outputs in parallel (SIPO configuration).

in the stack is the same as in the single switch, therefore ($C_{GS}\,R_{DS,on}$) product needs to improve faster than by multiplicative factor of $(1 + 1/N)^2$ by transferring to lower voltage processes when both conduction and gating loss is considered (assuming gate and conduction loss are close in value). When the complexity of maintaining voltage balance and gate driving is added, $N_{min} = N_{opt}$, unless there is another limitation on the actual part (e.g. power dissipation, temperature rise).

The cells' outputs need to be DC-isolated from their inputs, and either inductive or capacitive isolation is a valid option. In Appendix G, a two-stack implementation using the ISOR gate drive scheme with capacitive isolation was demonstrated. It is shown that balancing the input voltages of the individual cells is an issue that needs to be addressed for optimum performance. The method used in Appendix G provided voltage balancing within 2.2% ($\Delta V_{in} = 1.5$ V out of $V_{in} = 70$ V) relative to the input voltage, a result that is expected to be further improved with an active balancing technique. Since the converters are running at the same time, C_{in1} and C_{in2} theoretically need to be sized for ac currents drawn from the converters only since there is no additional energy storage requirement. It is expected however that the size needs to be an order of magnitude larger to provide stable operation, and is an issue of importance for the converters in a stack with independent control loops.

Inputs and outputs of the cells may be connected in different manners independently of each other, yielding four distinct configurations: PIPO, SISO, SIPO, PISO. Stacking is in theory not limited to only two cells. In practice, a challenge lies in implementing a control method capable of balancing multiple nodes, especially if the input voltage is not fixed (i.e. known a priori).

5.2 Modified Stack

Let us review the two-cell stack in Fig. 5.1. Suppose that the voltage transformation ratio of each cell is 1:1. If galvanic isolation is not required (LED lights, for example), the lower cell may be omitted completely without any impact on the upper cell. This observation motivated the configuration in Fig. 5.2. Clearly, input voltage distribution remained the same, but efficiency of the "lower cell" is increased to near 100%, thus improving the overall efficiency of the converter.

The technique is described in detail in Appendix H. The configuration where the input of the converter is connected in series with the load is derived from the SIPO stack and is termed "buck configuration", as the output voltage is always lower than the input voltage. A similar network, shown in Fig. 5.3, is derived from the PISO stack and is termed "boost configuration", as the output voltage is always higher than the input voltage. Note that C_{in2} in Fig. 5.2 and C_{out2} in Fig. 5.3 are redundant, however are kept in the schematic for clarity.

Fig. 5.4 shows a region of potential gains by using the buck configuration in V_{in} - P_{out} space, referenced to the original specifications of the converter. The region is bounded by not exceeding voltage and current stresses in the converter. If we strive to obtain higher power level by maintaining the same input voltage, the new input voltage of the inverter is $V'_{in} = V_{in} - V_{out}$. As a consequence, all voltage stresses in the inverter side are reduced by a factor of $V_{in}/V_{in}\prime$. Similarly, if we require higher output voltage but want to maintain the power level, the converter is scaled for lower output power accordingly.

SISO configuration is not possible as there is no path for the dc current in C_{in2}. PIPO stack leads to shorting input and output, therefore all control over the output voltage, current, or power flow is lost.

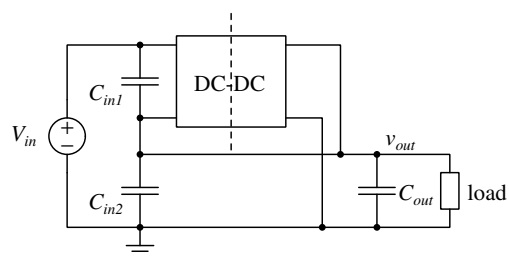

Figure 5.2: Modified single-cell stack with inputs in series and outputs in parallel ("buck configuration").

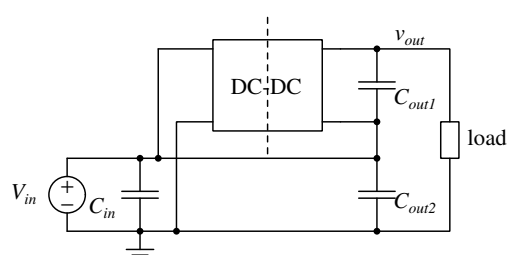

Figure 5.3: Modified single-cell stack with inputs in parallel and outputs in series ("boost configuration").

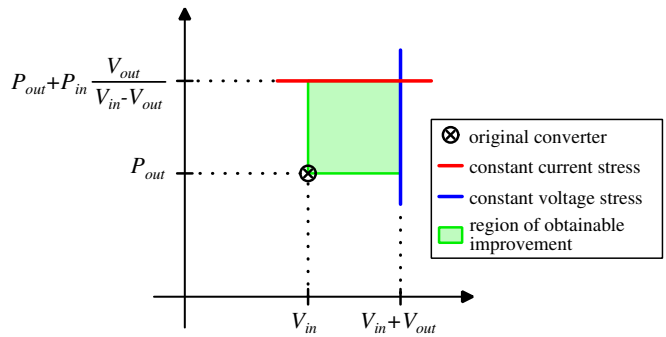

Figure 5.4: Modified single-cell stack, "buck" configuration: mapping of possible combinations of input voltage and output power in terms of V_{in}, V_{out}, P_{in}, and P_{out} of an unmodified converter, which do not exceed original voltage (blue) and current (red) stresses.

5.3 Design Considerations

The rectifiers in SIPO two-cell stack share the same ground, while the referent potentials of the inverters are connected via C_{in} capacitors, which are low impedance (dc blocking, ac short) elements at f_S. If the converters are capacitively isolated, it is necessary for the capacitors in the return paths to be low impedances as well. Otherwise there will be voltage across them - and if the converters are interleaved, the return currents are 180° out of phase, and resulting ac components of voltages across the capacitors to be 180° out of phase as well. As a result, the converters will interfere with each other and will operate in a non-optimal fashion. The situation is somewhat better if the converters are operated synchronously as the resulting voltages are in phase, which minimizes interaction between the converters. However, such voltage variation of the primary side ground input terminals can be a significant common-mode noise source, and it far easier to manage by using appropriately sized capacitors.

In SIPO type or buck type single-cell stack, voltage balancing across C_{in1} and C_{in2} capacitors prior to the converter start-up may need to be executed if the portion of the input voltage across the converter part to avoid excessive voltage across the switch. Care needs to be taken in certain applications where the load never decreases below standby power of the converter. A good example are LED applications, where this technique may be very useful depending on V_{out}/V_{in} ratio. By the time the LED leakage current gets to match the standby power of the converter (~10-100 μA), output voltage may drop by a factor of 2, depending on the diode size. Starting the converter with input voltage 1.5 higher than anticipated may easily exceed breakdown voltage limit and destroy the device.

5.4 Experimental Results

Appendix G presents ISOR SEPIC converter in SIPO configuration (see Fig. 5.5).

The 12 W converter was operated at 70 V input and 12 V output voltage, achieving 82% efficiency. When resistor dividers were used for bias voltage generation, the input voltage is was shared unequally by the power stage cells, with an offset of 1.5 V. The experiment was performed again with the use of 5 V linear regulators, and the voltage imbalance was reduced to 0.5 V (within 1.5% of $V_{in}/2$).

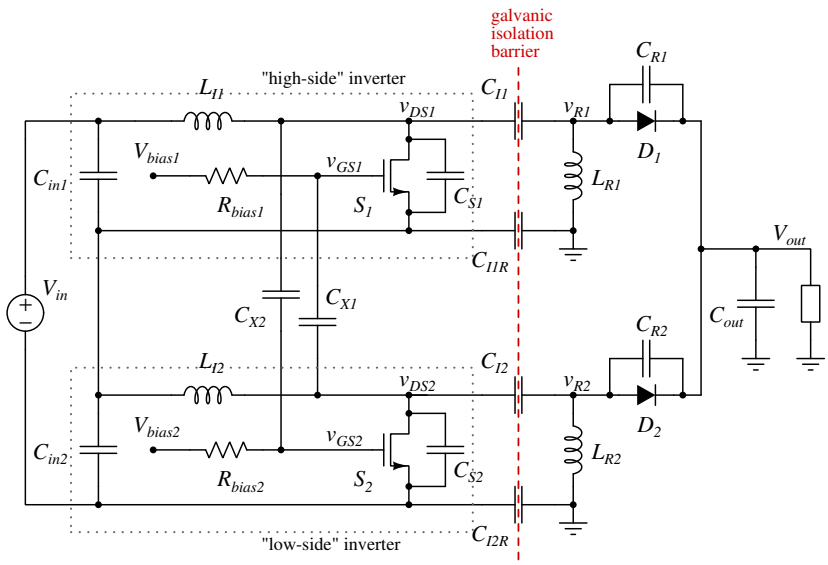

Figure 5.5: ISOR SEPIC power stage, SIPO configuration.

Appendix H shows ethe modified stack methodology, and its implementation on two off-the-shelf 12 V - 12 V converters (Murata NTE1212MC and CUI Inc. PDS1-S12-S12-S) and a resonant SEPIC converter. Efficiency was measured in unmodified and modified arrangements, and matched closely to the theoretical prediction.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

The work presented in this thesis and the associated publications addressed many facets of the overall problem of increasing the switching frequency of dc-dc converters into the VHF range. In the order of direct importance to the goal of providing affordable solutions with high efficiency, the major sub-contributions were:

- Low cost, high performance control scheme for self-oscillating gate drivers. Phase-shift self-oscillating (sliding mode) control found to be extremely well-suited for self-oscillating VHF dc-dc converters due to high tolerance to their inherent start-up and shut-down delays. The method demonstrated performance which rivals that of prior state-of-the-art. Behaviour of the proposed method in conjunction with VHF converters is modeled and experimentally verified.
- Modified stack power stage reconfiguration. Simple rearrangement of connections in a VHF power stage increases non-isolated VHF converter power level and efficiency for virtually no additional cost or penalty on power semiconductors.
- Self-oscillating gate drive method for multi-cell, class-E derived resonant converters with very low component count and gating loss. The method is experimentally demonstrated in several publications, with efficiencies of the prototypes being always above 80% at full load.
- Parallel-input and series-input two-cell configurations. High symmetry and balanced operation of the cells demonstrated experimentally.
- High converter performance using commercially available Si-based semiconductor devices. Most published work from this project is based on over-achieving semiconductor parts which were not intended to operate at VHF frequencies.

6.2 Perspectives on Future Research

The width of the covered topic resulted in significant improvements on the complexity, size, performance, and cost of VHF dc-dc power converters. As a side effect, there is a number of narrow topics which need addressing:

- Burst-mode control applied to stacked ISOR cells. In this work it is proven that ISOR cell stack can be made stable and share the input voltage. A two-cell stack design with burst mode control remains to be been implemented.
- Interleaved self-oscillating multi-resonant converter coupling. For multi-cell designs, the benefit of having only one extra capacitor per cell is very appealing. It is therefore of interest to look further into running the converters with multi-resonant network and lower peak voltage. The trade-off between number of stacked cells and efficiency needs to be investigated.
- Investigation of different self-oscillating schemes and their cooperation with phase-shift control. It is shown that phase-shift control scheme is robust and able to absorb delays from different sources in the feedback loop without discrimination. Most self-oscillating methods for VHF converters rely on usage of passive components and therefore have slow start-ups, and phase-shift control scheme is clearly a good, if not perfect, match with these methods.
- Digital/discrete-time phase-shift control. Continuous-time phase-shift control proved to be a strong competitor to popular hysteretic or PWM control methods. The amount of time-delay in digital circuits is comparable to those demonstrated in this work. Is it possible to implement high-performance feedback in discrete time domain?
- Investigation of GaN and SiC semiconductor devices. At the time of writing this thesis, GaN and SiC techonologies are in rapid development, with ever-improving switching performance.
- Optimization of Si-based semiconductor processes for VHF power conversion "friendliness". It is clear that most semiconductor processes are optimized without any regard to their VHF performance. In fact, most MOSFETs are optimized for hard-switched operation from few tens to few hundreds of kHz range. How would a MOSFET made in a process optimized for VHF dc-dc conversion look like?
- EMI characterization of converters with burst-mode control. This is an important issue since the on/off modulation frequencies and their higher harmonics typically lie in tens kHz to hundreds of kHz range, which is subjected to EMC compliance standards. What would it take for VHF converters to pass conducted and radiated EMI tests?

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Appendix A

On the Ongoing Evolution of Very High Frequency Power Supplies

IEEE Applied Power Electronics Conference and Exposition (APEC 2013, CA, USA)

On the Ongoing Evolution of Very High Frequency Power Supplies

Arnold Knott*, Toke M. Andersen*, Peter Kamby*, Mickey P. Madsen*, Milovan Kovacevic*, Michael A.E. Andersen*
*Technical University of Denmark
Ørsteds Plads, bygning 349
2800 Kongens Lyngby
Denmark
Email: akn@elektro.dtu.dk

***Abstract*—The ongoing demand for smaller and lighter power supplies is driving the motivation to increase the switching frequencies of power converters. Drastic increases however come along with new challenges, namely the increase of switching losses in all components. The application of power circuits used in radio frequency transmission equipment helps to overcome those. However those circuits were not designed to meet the same requirements as power converters. This paper summarizes the contributions in recent years in application of very high frequency (VHF) technologies in power electronics, describes the remaining challenges and shows results of the recent advances, among others a 120MHz, 9 W LED driver with 89 % efficiency.**

I. Introduction

The continuing trend of miniaturization in industrial and consumer electronics is continuously driving a demand for smaller power supplies. Weight and cost reduction demands accompany this trend. Within power supplies the major size, weight and cost drivers are typically the passive components. Increasing the switching frequency of power converters can reduce the size, weight and therefore the cost of those. For substantial size and weight reduction, the switching frequencies are increased up to the very high frequency (VHF) band (30 MHz to 300 MHz), which leads to a merge in circuit technologies used in radio frequency transmitters [1]–[6] and the classical power electronics circuits.

The VHF amplifiers are designed for DC-AC conversion, where the AC simultaneously is the switching frequency. Generally those circuits [1], [2] drive a known load impedance, typically a 50 Ω antenna. The most efficient standard representatives of radio frequency amplifiers are class-E [3], [4] and class-F [5], [6], where Class-E applies zero-voltage-switching (ZVS) and Class-F applies zero-current-switching (ZCS) techniques. Similarly to switch-mode power supplies, those VHF amplifiers convert the constant supply voltages into a high-frequent voltage by operating power semiconductors in the cut-off or saturation region only. The major difference is, that VHF amplifiers do not convert the energy back into a constant voltage or current level.

Numerous research works have been published [7]–[18], filling this gap and making VHF technologies available for power electronics. This paper describes the individual contributions of those in greater detail. However there are still some challenges left, before VHF switch-mode power supplies can relieve their advantages for products in industrial and consumer electronics.

This paper elaborates on the remaining challenges based on previous work and characterizes them in Section II. Section III describes the most recent advances, showing prototypes and measurement results. Section IV concludes the paper.

II. Challenges of VHF Converters

VHF operation of power supplies differs from sub-megahertz operated power supplies (here called traditional power converters) mainly by the following subjects:

- Electronic components, both active and passive,
- Circuit architectures for power stages and control parts,
- Adjacent behavior, such as electromagnetic compatibility (EMC) and mechanics.

A. Components

Especially inductive components are size, weight and cost optimization limitations in nowadays power circuits. Simultaneously VHF converters provide a major opportunity to overcome those.

Among the challenges are core losses, skin and proximity effect [19]–[25]. Another challenge within passive components for VHF is the creation of a galvanic isolation barrier [26], [27].

Despite passive components also active components, i.e. the power semiconductors, need to fulfill other requirements than in usual power supplies [28]–[30]. The parasitic components have a big influence on the design of the overall converter, as they are part of the design parameters. Unlike traditional power stages, the parasitic elements are therefore not considered undesired, but form an integral part of the stage. An example is the output capacitance C_{oss} of the power semiconductor in a Class-E based power supply. According to [17] it is dependent on output power P_{out}, input voltage V_{in} and switching frequency f_{sw} as shown in equation 1.

$$P_{out} = 2\pi^2 f_{sw} C_{oss} V_{in}^2 \tag{1}$$

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B. Architectures

Where traditional power electronics circuits use square wave gate drive signals, the presented VHF converters so far utilized sinusoidal gate drive [16], [31]–[33]. This is mainly due to the input capacitance C_{iss} of VHF power semiconductors, which require a high peak current at extremely high speed. To consider the drive trapezoidal, the rise and fall times have to be less than $1\ \mathrm{ns}$ [33]. A trapezoidal or square wave drive would minimize the time of the power switch in linear operation and therefore decreases the losses.

The degrees of freedom in terms of modulation principles are less for VHF converters. Whereas power electronics circuits usually use pulse width modulation or phase modulation, the VHF converters efficiency is dependent on those parameters. Therefore they need to be adjusted statically to avoid losses by leaving the ZVS (or ZCS) range. A way to get around this is to apply burst mode control [15], [31], [34]. This method however introduces another low frequency component in the spectrum, which has to be buffered or filtered at both the in- and output of the converter. A requirement that enforces the use of bulky components and therefore is counterproductive to the intended advantages of VHF converters in the first place. While the VHF converters offer good possibilities for fast transient regulations, their low frequency control performance is limited by intrinsic bandpass behaviors through serial capacitors. Even though some rectifiers are available with parallel capacitances and impedance transformation [17], [35], more suitable architectures are missing. Thereby it needs to be taken into account, that the original VHF power circuits are designed to match a defined load (typically the impedance of the antenna) and therefore impedance transformation circuits can be realized in a passive way. Power converters however are connected to highly varying loads, i.e. load circuit in idle - drawing no energy from the supply - and full load - demanding the maximum output from the supply. Therefore active and lossless impedance matching circuits are required. Having such circuits at hand opens for utilization of the high gain bandwidth in VHF converters for line and load regulation.

C. Adjacencies

Lastly the interaction of VHF converters with its physical environment is different than the one of traditional power converters.

On the one hand, the electromagnetic interaction between circuits increases, the higher the relevant frequencies are [36]–[39]. Fields are distributed easier both inside the converter and to its surroundings. The electrical behavior also becomes highly dependent on electromechanical interfaces, such as cooling and housing. However the harmonics of the resonant waveforms are falling faster, than the harmonics in hard switched traditional power converters [18]. Also the harmonics of the fundamental switching frequency are spaced wider. That means the distance can be used to place strategically important EMC bands, dependent on the application.

On the other hand, the carefully adjusted operating points of VHF converters (for efficiency purposes) are highly dependent on temperature [17], [18]. Adaptive mechanisms for ensuring optimal operation over industry standard temperature ranges are yet to come.

III. Recent Advances

Despite those challenges recent research results enhanced the state-of-the art in VHF converters and gives hope to overcome the remaining challenges.

The Class-E based power circuits allow for a second degree of soft switching. Despite turning the power switches on, when the voltage across them is zero (ZVS) or off, when the current through them is zero (ZCS), also the derivatives of these signals are taken into account. This is called ZdVS and ZdCS respectively. The technique has been applied to power converters in [17]. Figure 1 shows the full schematic of the power part of the self-oscillating VHF converter (DC-DC) from [17], [32].

Figure 2 shows the simulated waveforms of this converter, where v_s and i_s are the voltage and the current across and through the switch and v_D and i_D are voltage and current across and through the rectifier diode. v_G is the control signal of the power switch and V_o and V_i are input and output voltages of the converter. The top graph v_s visualizes the optimization of the converter for both ZVS and ZdVS.

Figure 3 is a photograph of the implementation of this converter. The overall efficiency of the $97\ \mathrm{MHz}$ converter is $55\ \%$.

Due to the tight adjustment of the turn on instance of the power switch for achieving ZVS and ZdVS the degrees of freedom in this converter are low. That limits the input and output voltage ranges. Furthermore the efficiency is not acceptable. In this case, the majority of the losses are due to conduction losses in the power semiconductors.

Suboptimal operation of Class-E converters as described in [4] opened for higher degrees of freedom in the design of Class-E based DC-DC converters. This means, that the ZdVS condition is only fulfilled under nominal load conditions and only ZVS is fulfilled otherwise. The effects of these operation mode as described in [40] has been extended in [18] to LED lighting applications.

Furthermore [18] provides a detailed analysis of the power components parasitics and the effect of their nonlinearities. The most relevant parasitics of the power switch are the input and output capacitances. They are typically highly nonlinear. Figure 4 shows the relative voltage stress of the power switch

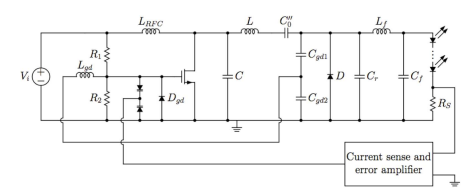


Fig. 1: Complete schematic of a self-oscillating VHF converter [32] with LED load.

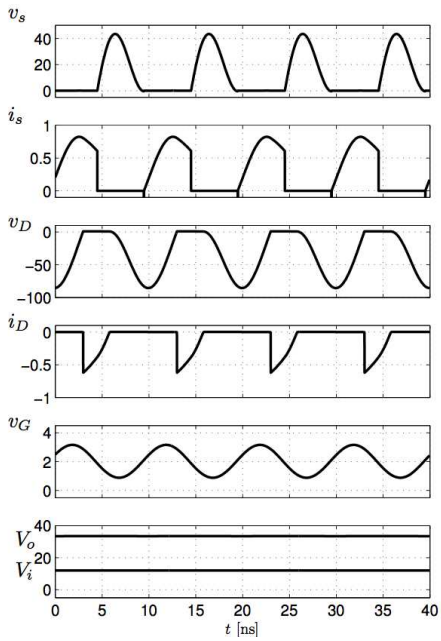


Fig. 2: Simulation of waveforms for a ZVS and ZdVS Class-E based converter from [17].

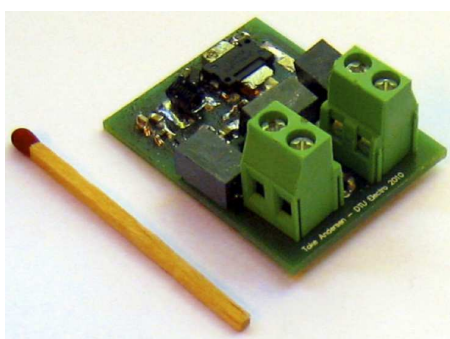


Fig. 3: Photograph of the self-oscillating VHF converter from [32].

as a function of time and junction potential.

The other components of the power stage have been investigated in [18] as well. Thereby most focus is on the inductors, as these are the most volume consuming parts, have the biggest weight and typically a big impact on the overall price of the converter. Therefore the inductors have been integrated as toroids into the printed circuit board (PCB). This process

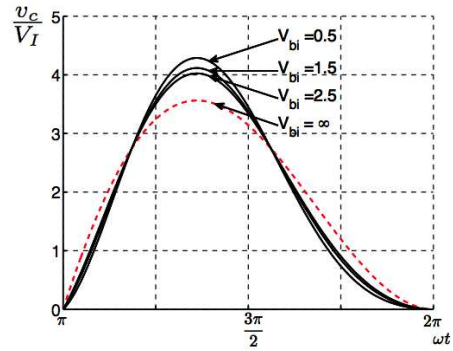


Fig. 4: Voltage stress of the power switch in relation to DC input voltage for a nonlinear output capacitance from [18]. V_{bi} is the junction potential of the process.

is described in [41] and Figure 5 shows the principle.

The resulting converter waveform in the optimal and suboptimal operating regions are shown in Figure 6. The converters efficiency is in the same area as the previous presented. For dealing with the efficiency challenge, [42] compared a number of power switches both in simulation and experiment. Figure 7 shows photographs of the implementations. On top of that an effective line- and load regulation scheme was implemented in those.

Figure 8 shows the implementation of the final prototype with 70 MHz switching frequency. The voltage step-down ratio of the converters is 10 and the output power range is between 1

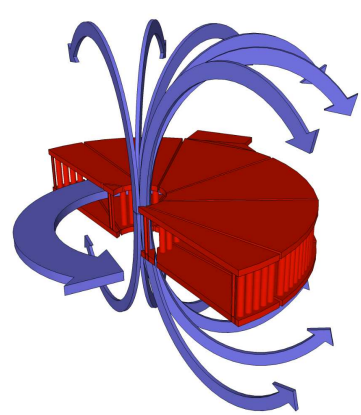
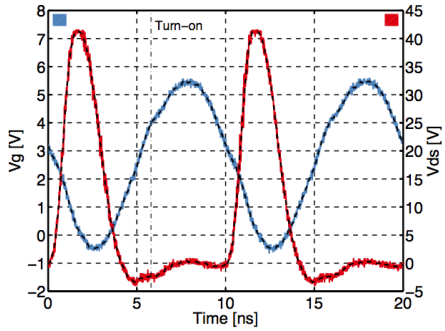
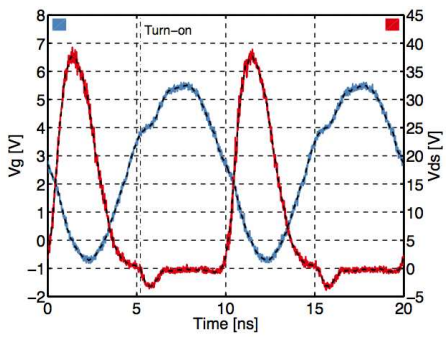


Fig. 5: PCB integrated inductor from [41]. The copper contained in the PCB is shown in red. The blue arrows mark the magnetic field.



(a) optimal operation



(b) suboptimal operation

Fig. 6: Measurements of gate-source and drain-source voltages V_{gs} and V_{ds} of the power switch and the turn-on instances. Note that the drain-source voltage has an offset of -0.5 V, due to the oscilloscopes offset.

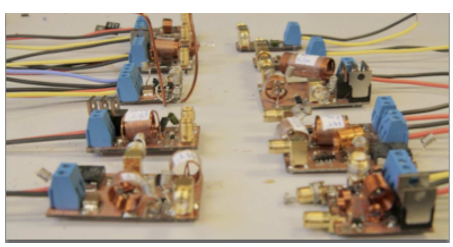


Fig. 7: Photograph of numerous prototypes for comparing measured efficiency with simulations [42].

and 4W at an efficiency within this range beyond 70 %.

Additionally the self-oscillating principle from [17], [32] was applied to an interleaved Class-E converter in [43], resulting into a significant efficiency improvement. The complete schematic is shown in Figure 9. The realized converter is switching at 120 MHz, i.e. beyond the FM band, converts

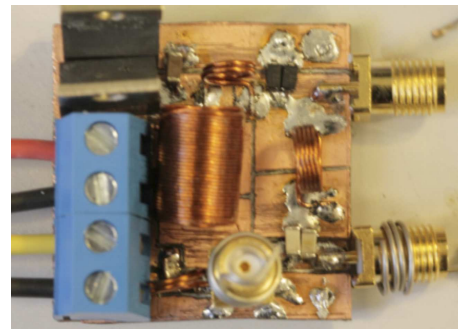


Fig. 8: Photograph of a closed loop low-power VHF converter with an efficiency beyond 70 % from [42]. The TO220 components on the upper left is the dummy load resistance.

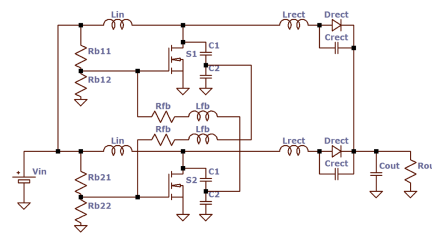


Fig. 9: Full schematic of interleaved Class-E converter from [43].

an input voltage between 6 and 9 V into an output current between 0.4 and 0.5 A and has an efficiency between 80 and 89 % within this operation range. The output power range is 3 to 9 W and the converter is built for LED drive. Figure 10 shows both a SPICE based simulation and a the measurement of the power switches voltage waveforms.

IV. Conclusion

The merge of techniques used in radio communication electronics and power electronics was pointed out. The development through the previous decades has been revisited and recent developments were summarized. Remaining challenges and the latest advances were described. The implementations of numerous VHF converters were presented. Among them are low-power, high-step-down converters with a switching frequency of 70 MHz and an efficiency beyond 70 % as well as a 120 MHz, 9 W LED driver with an efficiency up to 89 %. Both converters maintain high efficiencies over a wide load range.

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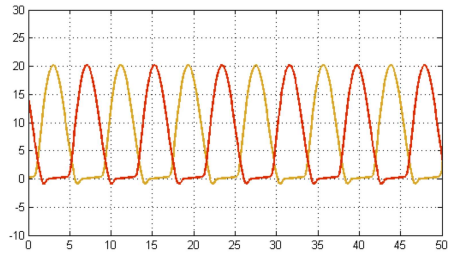
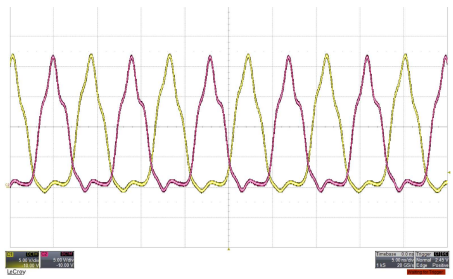


(a) simulated waveforms



(b) measured waveforms

Fig. 10: Drain-source waveforms of the two power switches in the interleaved converter from [43].

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Appendix B

Evolution of Very High Frequency Power Supplies

IEEE Journal of Emerging and Selected Topics in Power Electronics

Evolution of Very High Frequency Power Supplies

Arnold Knott, *Member, IEEE*, Toke M. Andersen, *Student Member, IEEE*, Peter Kamby, Jeppe A. Pedersen, Mickey P. Madsen, *Student Member, IEEE*, Milovan Kovacevic, *Student Member, IEEE*, and Michael A. E. Andersen, *Member, IEEE*

***Abstract*— The ongoing demand for smaller and lighter power supplies is driving the motivation to increase the switching frequencies of power converters. Drastic increases however, come along with new challenges, namely the increase of switching losses in all components. The application of power circuits used in radio frequency transmission equipment helps to overcome those. However, those circuits were not designed to meet the same requirements as power converters. This paper summarizes the contributions in the recent years in the application of very high frequency (VHF) technologies in power electronics, which show the results of the recent advances and describes the remaining challenges. The presented results include a self-oscillating gate drive, air-core inductor optimizations, an offline LED driver with a power density of 8.9 W/cm^3, and a 120-MHz, 9-W dc powered LED driver with 89% efficiency as well as a bidirectional VHF converter. The challenges to be solved before VHF converters can be used effectively in industrial products are within those three categories: 1) components; 2) circuit architectures; and 3) reliability testing.**

***Index Terms*— DC–DC power converters, power conversion, resonant inverters, very high frequency (VHF) circuits, zero-voltage switching (ZVS).**

I. Introduction

THE continuing trend of miniaturization in industrial and consumer electronics is continuously driving a demand for smaller power supplies. Weight and cost reduction demands accompany this trend. Within power supplies, the major size, weight, and cost drivers are typically the passive components. Increasing the switching frequency of power converters can reduce the size, weight, and therefore the cost of those. For substantial size and weight reduction, the switching frequencies are increased up to the very high frequency (VHF) band (30–300 MHz), which leads to a merge in circuit technologies used in radio frequency transmitters [1]–[6] and the classical power electronics circuits.

The VHF amplifiers are designed for dc–ac conversion, where the ac simultaneously is the switching frequency. Generally, those circuits [1], [2] drive a known load impedance, typically a $50-\Omega$ antenna. Traditionally, the topologies used for those circuits have been characterized as classes with running labels following the alphabet. Class-A, B, and C are described in [7] and [2]. These classes are characterized through the relative amount of time; the power transistor is conducting the load current with respect to the period of the VHF signal. For class-A, the transistor conducts the load current 50% of the time. Class-B operates between 25% and 50% and class-C between 0% and 25%. This leads to theoretical maximum achievable efficiencies of 50%, up to 78.5%, and up to 100% for class-A, B, and C, respectively. Their power electronics counter parts are linear regulators. Class-D is described in [8] and the first power circuit topology, which allows for theoretical 100% efficiency under all operating conditions. The equivalent is strictly all hard-switched power converters. Class-E, as described in [3] and [4], and class-F, as demonstrated in [5] and [6], correspond to all power converters, that apply zero-voltage switching (ZVS) and zero-current switching (ZCS) techniques, respectively.

Similar to switch-mode power supplies, those VHF amplifiers convert the constant supply voltages into a high-frequent voltage by operating power semiconductors in the triode region only. The major difference is that VHF amplifiers do not convert the energy back into a constant voltage or current level.

Numerous research works have been published [9]–[20], filling this gap and making VHF technologies available for power electronics. This paper describes the individual contributions of those in greater detail. However, there are still some challenges left, before VHF switch-mode power supplies can relieve their advantages for products in industrial and consumer electronics.

This paper elaborates on the most recent advances, showing prototypes and measurement results in Section II. Section III describes the remaining challenges based on previous work and characterizes them. Section IV concludes this paper.

II. Recent Advances

Recent research results enhanced the state of the art in VHF converters. Most of the works in the recent years have focused on class-E derived topologies.

A. Optimal Operation

The class-E-based power circuits allow for a second degree of soft switching. Despite turning the power switches on, when the voltage across them is zero (ZVS), also the derivatives of these signals are considered. This is called ZdVS and ZdCS, respectively. The technique has been applied to power converters in [19]. The schematic diagram in Fig. 1 shows the

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The authors are with the Technical University of Denmark, Kgs, Lyngby 2800, Denmark (e-mail: akn@elektro.dtu.dk; andersen@lem.ee.ethz.ch; peter@kamby.dk; jarpe@elektro.dtu.dk; mpma@elektro.dtu.dk; mikov@elektro.dtu.dk; ma@elektro.dtu.dk).

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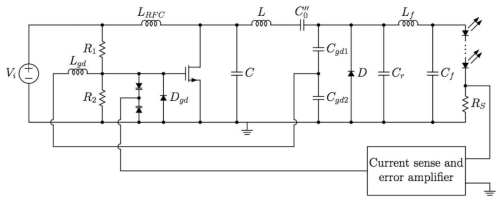

Fig. 1. Schematic diagram of a self-oscillating VHF converter [24] with LED load.

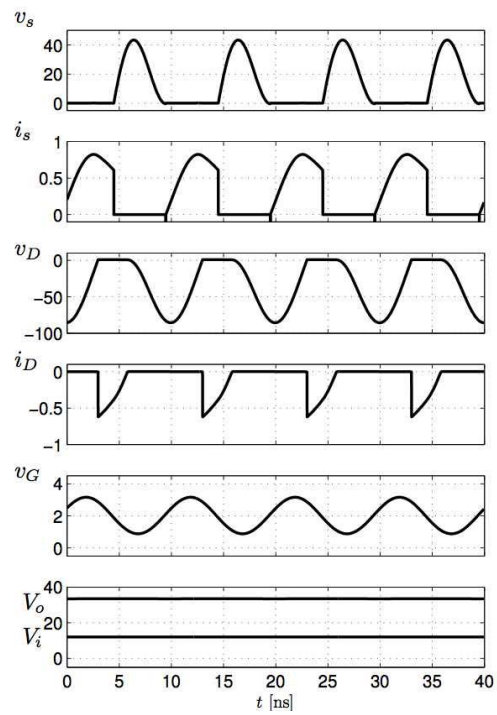

Fig. 2. Simulated waveforms for an ZVS and ZdVS class-E-based converter from [19].

adoption of the principles of a class-E oscillator, e.g., shown in [21]–[23], to a class-E-based power self-oscillating VHF converter (dc–dc) [19], [24]. A converter achieving both ZVS and ZdVS at all times operates in optimal mode.

Other implementation replaced either the resonant tank [25], [26] or the input inductor [11], [27] with a transmission line. The resulting waveforms of this circuit have been reported in, e.g., [28]–[33] and Fig. 2 shows the simulated waveforms of this converter, where v_s and i_s are the voltage and the current across and through the switch and v_D and i_D are voltage and current across and through the rectifier diode. v_G is the control signal of the power switch and V_o and V_i are input and output voltages of the converter. The top graph v_s shows the optimization of the converter for both ZVS and ZdVS.

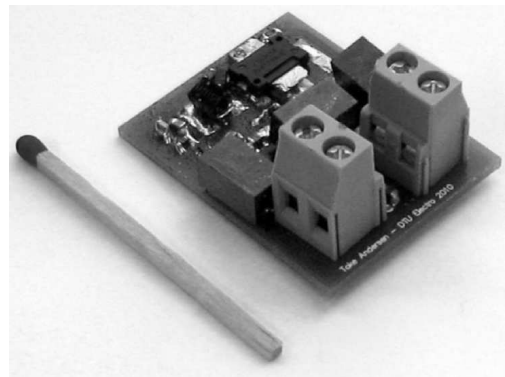

Fig. 3. Photograph of the self-oscillating VHF converter from [24].

Fig. 3 shows a photograph of the implementation of this converter. The overall efficiency of the 97-MHz converter is 55%.

The advantage of this converter is that it is based on a widely documented circuit topology from the communication electronics applications. As implemented here, it also provides means of output regulation. The downside is the voltage stress across the power switch, 3.6 times higher as in hard-switched converters.

B. Suboptimal Operation

Due to the tight adjustment of the turn-on instance of the power switch for achieving ZVS and ZdVS the degrees of freedom in this converter are low. That limits the input and output voltage ranges. Furthermore, the efficiency is not acceptable. In this case, the majority of the losses are due to conduction losses in the power semiconductors, which are due to the on-resistance of the power switch. As the gate voltage is not significantly higher than the threshold voltage, the devices minimum on-resistance could not be achieved.

Suboptimal operation of class-E converters, as described in [4], opened for higher degrees of freedom in the design of class-E-based dc–dc converters. This means that the ZdVS condition is only fulfilled under nominal load conditions and only ZVS is fulfilled otherwise. The resulting converter waveform in the optimal and suboptimal operating regions is shown in Fig. 4. The effects of these operation mode, as described in [34], have been extended in [20] to LED lighting applications.

Note that the body diode of the MOSFET is conducting in the beginning of the MOSFETs conduction period. This is due to wrong timing in the turn-on of the power device. The energy lost in the body diode ruins the efficiency of this particular converter.

Furthermore, [20] provides a detailed analysis of the power components parasitics and the effect of their nonlinearities. The basis for this analysis has been, among others, laid in [35] and [36] for the analysis of class-E amplifiers, which is fully applicable to class-E-based power converters when

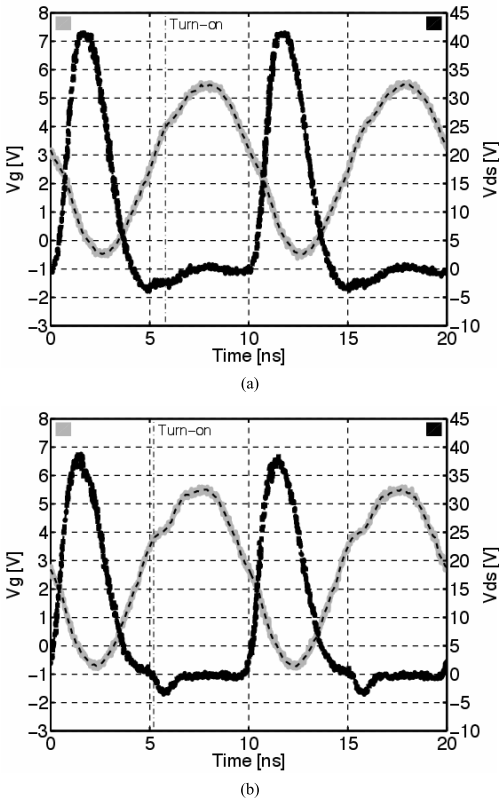

Fig. 4. Measurements of gate-source and drain-source voltages $V_{\rm gs}$ and $V_{\rm ds}$ of the power switch and the turn-on instances. Note that the drain–source voltage has an offset of −0.5 V, due to the oscilloscopes offset. (a) Optimal operation. (b) Suboptimal operation.

tuning the rectifier to act as an ohmic load. The most relevant parasitics of the power switch are the input and output capacitances. The later is the most critical for the design of the converter. Simultaneously, the output capacitance is highly nonlinear, which was considered in the analysis in [20]. There, the nonlinearity of the output capacitance $C_{\rm ds}$ is modeled with

$$C_{\rm ds}(V_c) = \frac{C_{j0}}{\left(1+\frac{V_c}{V_{\rm bi}}\right)^{\gamma}} \tag{1}$$

where C_{j0} is the junction capacitance at 0 V, $V_{\rm bi}$ is the built-in junction potential, typically 0.5–0.9 V [29], and γ is the junction sensitivity or gradual coefficient. Typically, $\gamma = 1/3$ for gradient junctions, while $\gamma = 0.5$ for abrupt junctions [1] hence junction diodes [29], and v is the junction voltage.

This results in a voltage waveform V_c of the power switch as a function of the converters input current $I_{\rm in}$ and the above

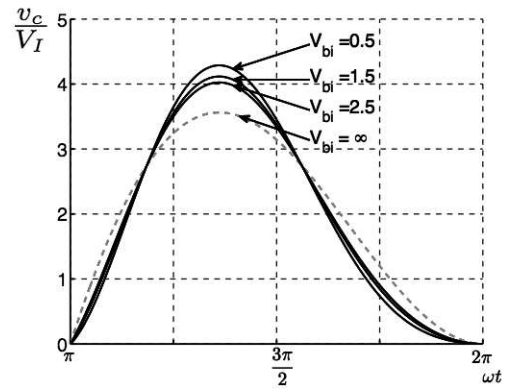

Fig. 5. Voltage waveform of the power switch in relation to dc input voltage for a nonlinear output capacitance from [20]. $V_{\rm bi}$ is the junction potential of the process.

output capacitances parameters as

$$V_c = V_{\rm bi}\left(\left[\frac{I_{\rm in}(1-\gamma)}{\omega C_{j0} V_{\rm bi}} \times \left(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t\right) + 1\right]^{\frac{1}{1-\gamma}} - 1\right). \tag{2}$$

Fig. 5 shows the relative voltage waveform of the power switch as a function of time and junction potential $V_{\rm bi}$ for a junction sensitivity of $\gamma = 0.5$.

The remaining components of the power stage have been investigated in [20] as well. Thereby, most focus is on the inductors, as these are the most volume-consuming parts, have the biggest weight and typically a big impact on the overall price of the converter. Therefore, the inductors have been integrated as toroids into the printed circuit board (PCB). This process is described in [37] and Fig. 6 shows the principle.

A power stage has been designed to operate in suboptimal mode under the consideration of the power switches nonlinear output capacitance. The converters efficiency is in the same area as the one presented in Section II-A and again limited by a high on-resistance, which is due to a low gate drive voltage. While giving up on the single operating point operation in optimal operation mode, the suboptimal operating converters theoretically allow for different conduction angle operation on the cost of tighter timing to operate in ZVS.

C. Class-E-Based SEPIC Converter

For dealing with the efficiency challenge, [38] compared a number of power switches both in simulation and experiment. Furthermore, multiple air-core inductors where calculated, designed, and implemented. An extraction is shown in Fig. 8. The prototypes reach Q-values beyond 100 and resonance frequencies up to 340 MHz. Fig. 9 shows a photograph of the implemented converters. On top of that, an effective line and load regulation scheme was realized in those. The designs where verified in a SEPIC converter (Fig. 7) [39], based on

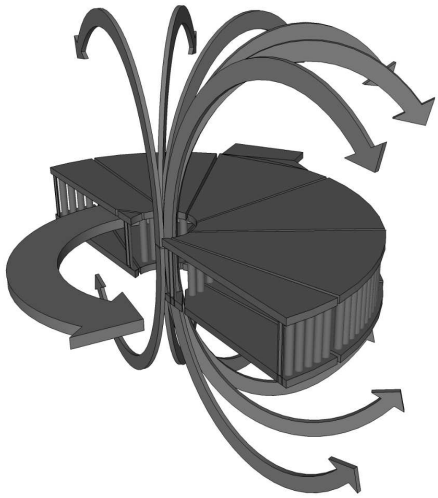

Fig. 6. PCB integrated inductor from [37]. The cross section of the PCB toroid and the resulting flux arrows are shown.

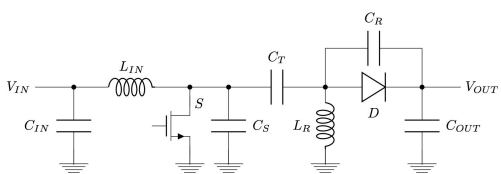

Fig. 7. Schematic diagram of a class-E-based SEPIC VHF converter [39].

Fig. 8. Photograph of various air-core inductors [38].

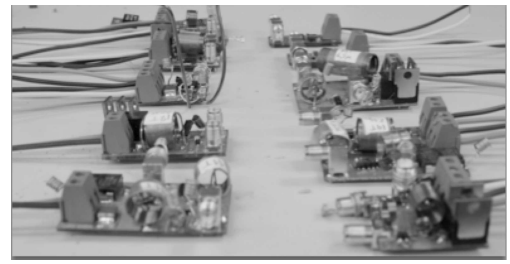

Fig. 9. Photograph of numerous prototypes for comparing measured efficiency with simulations [38].

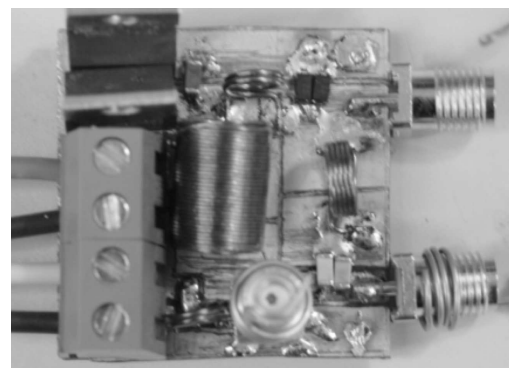

Fig. 10. Photograph of a closed loop low-power VHF converter with an efficiency beyond 70% from [38]. The TO220 components in the upper left corner are the dummy load resistance.

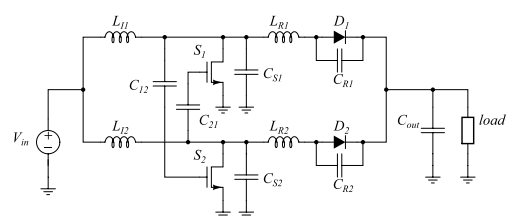

Fig. 11. Full schematic view of the open-loop interleaved class-E converter from [43].

the topologies presented in [40], achieving a power density of 8.9 W/cm^3 (146 W/in^3) by switching at 51 MHz for offline LED applications.

Fig. 10 shows the implementation of the final prototype with 70-MHz switching frequency. The voltage step-down ratio of the converters is 10 and the output power range is between 1 and 4 W at an efficiency within this range beyond 70%.

Compared with the above-reported converters, the SEPIC converter is not based on an inverter that delivers a sinusoidal output. The later is crucial in telecommunication applications, when using the class-E inverter as a transmitter, but completely unnecessary demand as an intermediate VHF link within a dc/dc power converter. Relaxing this requirement removes the resonant tank inductor, and therefore the resonant tanks bandpass behavior. On the other hand, the rectifier can no longer freely be chosen between several topologies, but has to be implemented with a diode, not referenced to ground, which is a disadvantage in some implementation technologies, such as integrated circuits.

D. Interleaved VHF Converters

In addition, the self-oscillating principle from [19] and [24] was combined with the interleave principle from [41] and [42] in [43], resulting into a significant efficiency improvement. Interleaving two converter legs allows furthermore to use the ripple cancelation, as described in [44] and applied in [41]. The complete schematic diagram of the open-loop implementation is shown in Fig. 11. The realized converter

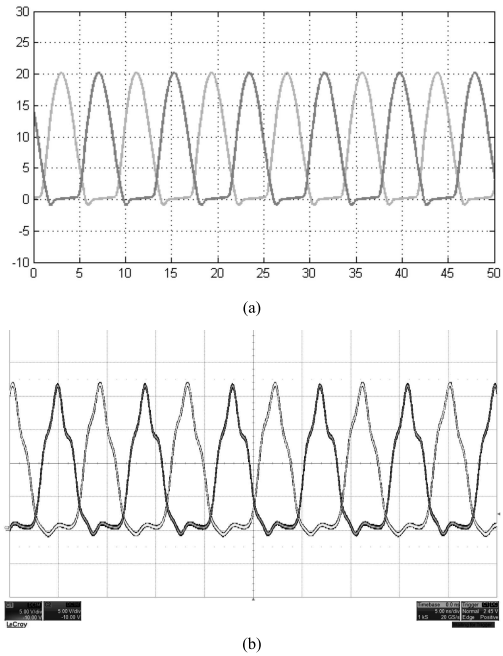

Fig. 12. Drain–source waveforms of the two power switches in the interleaved converter from [43]. (a) Simulated waveforms. (b) Measured waveforms.

is switching at 120 MHz, i.e., beyond the FM band, converts an input voltage between 6 and 9 V into an output current between 0.4 and 0.5 A and has an efficiency between 80 and 89% within this operation range. The output power range is 3–9 W, corresponding to an output voltage range between 7 and 20 V. The converter is designed to drive LEDs. Fig. 12 shows both a SPICE-based simulation and the measurement of the power switches voltage waveforms. Fig. 13 shows the efficiency graph of this converter.

Interleaved converters allow for input and/or output ripple cancellation, segmented power stages, which enables higher power levels [45]. However, those converters suffer from different optimal frequencies due to tolerances for each leg, which either might result in beat tones, when operating each of them at its own optimal resonant frequencies, or a nonoptimal operation point with respect to efficiency for all legs, when operating all legs at the same frequency.

E. Bidirectional VHF Converter

Replacing the diode in Fig. 1 with a transistor, the class-E amplifier and the class-E synchronous rectifier form a symmetric schematic view, as shown in Fig. 14. This was realized in [46] and resulted in a bidirectional converter with the same conversion ration from both sides. Operating in the forward mode, the transistor M_1 is the power switch, operating in class-E mode, and M_2 is used as synchronous rectifier in class-E operation. In the reverse operating mode, the voltage

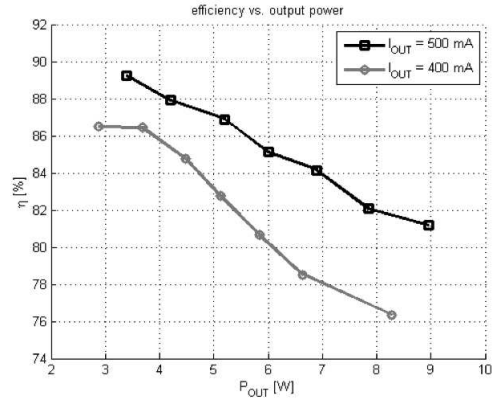

Fig. 13. Efficiency of a battery driven LED driver switching at 120 MHz [43].

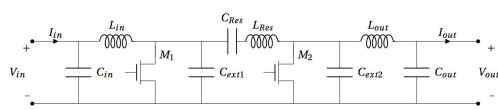

Fig. 14. Schematic diagram of a VHF converter with class-E inverter and synchronous class-E rectifier [46].

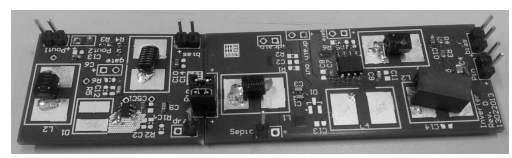

Fig. 15. Photograph of a bidirectional VHF converter [46].

designated V_{out} is acting as the input voltage and M_2 becomes the inverter switch, while M_1 turns into the synchronous rectifier. The maximum achieved efficiency with this topology was 70% switching at 30 MHz. A photograph of the prototype and thermal pictures of the converter are shown in Figs. 15 and 16, respectively. The bidirectional converter allows for lower conduction losses in the rectifier and allows for two-quadrant operation at the cost of an extra gate, which needs a control signal.

III. Challenges of VHF Converters

Lately, remaining research challenges have been described in [47] and [48]. This section summarizes the remaining challenges common in all above-described converters with respect to implementation in products. It is dividing the major remaining show stoppers into three categories and describes those afterward with respect to the existing products on the power supply market, with switching frequencies below the VHF range.

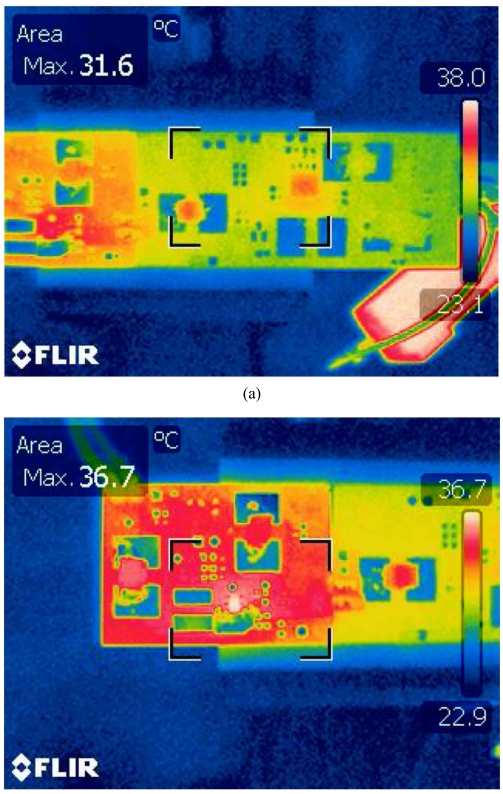

Fig. 16. Thermal photographs of bidirectional VHF converter in thermal equilibrium [46]. (a) Class-E inverter. (b) Class-E synchronous rectifier.

VHF operation of power supplies differs from submegahertz operated power supplies (here called traditional power converters) mainly by the following subjects:

1) electronic components, both active and passive;
2) circuit architectures for power stages and control parts;
3) adjacent behavior, such as electromagnetic compatibility (EMC), mechanics, and other reliability tests.

A. Components

Especially, inductive components are size, weight, and cost optimization limitations in nowadays power circuits. Simultaneously, VHF converters provide a major opportunity to overcome those.

Among the challenges are core losses, skin, and proximity effect [27], [49]–[54]. For driving further miniaturization of VHF power supplies, an obvious next step is to integrate the whole converter in a package (power supply in package) or even on a single chip (power supply on chip). The most challenging part for this goal is the integration of the inductors. Great progress has been made and summarized lately in [55], [56]. However, realizations of integrated inductors with Q-values beyond 100 in the relevant frequency ranges remain to be seen. Hybrid concepts, as shown in [57], might be applicable. Another challenge within passive components for VHF is the creation of a galvanic isolation barrier [58]–[60].

Despite passive components also active components, i.e., the power semiconductors, need to fulfill other requirements than in usual power supplies [61]–[63]. The parasitic components have a big influence on the design of the overall converter, as they are a part of the design parameters. Unlike traditional power stages, the parasitic elements are therefore not considered undesired, but form an integral part of the stage. An example is the output capacitance C_{oss} of the power semiconductor in a class-E-based power supply. According to [19], it is dependent on output power P_{out}, input voltage V_{in}, and switching frequency f_{sw}, as

$$P_{\mathrm{out}} = 2\pi^2 f_{\mathrm{sw}} C_{\mathrm{oss}} V_{\mathrm{in}}^2. \tag{3}$$

This means that the output capacitance C_{oss} limits the maximum switching frequency for a given application, which specifies P_{out} and V_{in}.

B. Architectures

Where traditional power electronics circuits use square-wave gate drive signals, the presented VHF converters so far used sinusoidal gate drive [18], [24], [64], [65]. This is mainly due to the input capacitance C_{iss} of VHF power semiconductors, which require a high peak current at extremely high speed. To consider the drive voltage trapezoidal, its rise and fall times have to be less than 1 ns [65]. A trapezoidal or square-wave drive would minimize the time of the power switch in linear operation and therefore decreases the losses. The degrees of freedom in terms of modulation principles are less for VHF converters. Whereas power electronic circuits usually use pulsewidth modulation or phase modulation, the VHF converter efficiency is dependent on those parameters. Therefore, they need to be adjusted statically to avoid losses by leaving the ZVS (or ZCS) range. A way to get around this is to apply burst mode control [17], [64], [66]. This method, however, introduces another low-frequency component in the spectrum, which has to be buffered or filtered at both the in and output of the converter. A requirement that enforces the use of bulky components and therefore is counterproductive to the intended advantages of VHF converters in the first place. While the VHF converters offer good possibilities for fast transient regulations, their low-frequency control performance is limited by intrinsic bandpass behaviors through serial capacitors. Even though some rectifiers are available with parallel capacitances and impedance transformation [19], [67], more suitable architectures are missing. Thereby, it needs to be considered that the original VHF power circuits are designed to match a defined load (typically the impedance of the antenna), and therefore impedance transformation circuits can be realized in a passive way. Power converters however, are connected to highly varying loads, i.e., load circuit in idle—drawing no energy from the supply and full load—demanding the maximum output from the supply. Therefore, active and lossless impedance matching circuits are required.

Having such circuits at hand opens for the utilization of the high gain bandwidth in VHF converters for line and load regulation.

C. Adjacencies

Finally, the interaction of VHF converters with its physical environment is different than the one of traditional power converters.

On the one hand, the electromagnetic interaction between circuits increases, the higher the relevant frequencies are [68]–[71]. Fields are distributed easier both inside the converter and to its surroundings. The electrical behavior also becomes highly dependent on electromechanical interfaces, such as cooling and housing. However, the harmonics of the resonant waveforms are falling faster than the harmonics in hard switched traditional power converters [20]. In addition, the harmonics of the fundamental switching frequency are spaced wider. That means the distance can be used to place strategically important EMC bands, dependent on the application.

On the other hand, the carefully adjusted operating points of VHF converters (for efficiency purposes) are highly dependent on temperature [19], [20]. Adaptive mechanisms for ensuring optimal operation over industry standard temperature ranges are yet to come.

IV. Conclusion

The merge of techniques used in radio communication electronics and power electronics was pointed out. The development through the previous decades has been revisited and the recent developments were summarized. Remaining challenges and the latest advances were described. The implementations of numerous VHF converters were presented. Among them are low-power, high-step-down converters with a switching frequency of 70 MHz and an efficiency beyond 70% as well as a 120-MHz, 9-W LED driver with an efficiency up to 89%. Both converters maintain high efficiencies over a wide load range.

The remaining challenges that require solutions before VHF converters can be implemented in numerous industrial applications were found to be within the categorizes components, circuit architectures, and reliability testing.

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Arnold Knott (M'10) received the Diplom-Ingenieur degree from the University of Applied Sciences, Deggendorf, Germany, in 2004, and the Ph.D. degree from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2010.

He has been with Harman/Becker Automotive Systems GmbH in Germany and USA, from 2004 to 2009, designing switch-mode audio power amplifiers and power supplies for automotive applications. He is involved in a research project under the title "Improvement of out-of-band Behaviour in Switch-Mode Amplifiers and Power Supplies by their Modulation Topology." From 2010 to 2013, he was an Assistant Professor and an Associate Professor with the Technical University of Denmark since 2013. His current research interests include switch-mode audio power amplifiers, power supplies, active and passive components, integrated circuit design, acoustics, radio frequency electronics, electromagnetic compatibility, and communication systems.

Toke M. Andersen (S'10) received the B.Sc. and M.Sc. degrees from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2008 and 2010, respectively. He is currently pursuing the Ph.D. degree with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology Zürich, Zürich, Switzerland, in collaboration with IBM Research Zurich, Rüschlikon, Switzerland.

His current research interests include analysis, design, implementation, and optimization of on-chip power converters in deep submicrometer CMOS technologies.

Peter Kamby received the B.Sc. and M.Sc. degrees from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2009 and 2012, respectively.

His current research interests include very high frequency switch-mode power supplies, high current power conversion, and pulsed power.

Jeppe A. Pedersen received the B.Sc. and M.Sc. degrees from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2010 and 2013, respectively.

He is currently a Research Assistant with the Technical University of Denmark. His current research interests include very high frequency switch-mode power supplies, bidirectional power conversion, and light-emitting diode drivers.

Mickey P. Madsen (S'12) received the B.Sc.E.E. and M.Sc.E.E. degrees from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2009 and 2012, respectively. He is currently pursuing the Ph.D. degree in power electronics under the title "Very High Frequency Switch Mode Power Supplies."

His current research interests include switch-mode power supplies, resonant inverters/converters, wide band gab semiconductors, solid state (LED) lighting, and radio frequency electronics.

Milovan Kovacevic (S'13) received the B.Sc. and M.Sc. degrees from the University of Belgrade, Belgrade, Serbia, in 2008 and 2010, respectively. He is currently pursuing the Ph.D. degree with the Department of Electrical Engineering, Technical University of Denmark, Kongens Lyngby, Denmark.

His current research interests include high-frequency power electronics, resonant and soft-switching techniques, analog and mixed-signal circuit design, and control of power converters.

Michael A. E. Andersen (M'88) received the M.Sc.E.E. and Ph.D. degrees in power electronics from the Technical University of Denmark, Kongens Lyngby, Denmark, in 1987 and 1990, respectively.

He is currently a Professor of power electronics with the Technical University of Denmark. Since 2009, he has been the Deputy Director with the Department of Electrical Engineering. He is the author or coauthor of more than 200 publications. His current research interests include switch-mode power supplies, piezoelectric transformers, power factor correction, and switch-mode audio power amplifiers.

Appendix C

Interleaved Self-Oscillating Class E Derived Resonant DC-DC Converters

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Interleaved Self-Oscillating Class E Derived Resonant DC/DC Converters

Milovan Kovacevic, Arnold Knott, Michael A. E. Andersen
Technical University of Denmark, Department of Electrical Engineering
Oersteds Plads Building 349, Lyngby, Denmark
mikov@elektro.dtu.dk; akn@elektro.dtu.dk; ma@elektro.dtu.dk

Abstract – A new method for achieving self-oscillating, self-interleaved operation of class E derived resonant DC/DC converters is presented. The proposed method is suitable for operation at frequencies in the Very High Frequency (VHF) band. Interleaved and self-oscillating modes of operation are achieved at the same time with very small number of additional passive components in the interconnection network. To verify the proposed technique, a 110MHz prototype resonant boost converter was designed; experimental results and comparison with SPICE simulation are presented. Peak measured efficiency was 89% in continuous operation.

***Keywords*:** resonant DC/DC converter, class E inverter, very high frequency, interleaved, self-oscillating converter

1. Introduction

Increase of switching frequency of DC/DC converters has significant benefits – size reduction of energy storage elements, faster transient response, reduction in system cost, possibility of integration of power converters in places normally unfit for such devices, and EMI performance. Since reactive components (especially inductors and transformers) are in most cases the major contributors to converter size, increase of switching frequency allow for smaller storage elements, both in physical size and value (Rivas et al., 2006a, Perreault et al., 2009). In case of inductors and transformers, the use of magnetic core may be avoided, which eliminates magnetic core losses in converters.

On the other hand, increase of operating frequency causes rapid rise of switching and gating losses to unacceptable levels in hard switching topologies, as shown by Rivas et al. (2006a). In case of very high frequencies (VHF), difficulties in design of a high side driver impose further constraints on topology selection. This requires careful gate driver design.

One possibility to address this issue is to design the converter to be self-oscillating, as proposed by Kazimierczuk et al. (2005) and Andersen et al. (2011). In these reports, self-oscillating operation is achieved via feedback loop within the inverter stage. Self-oscillating resonant converters are suitable for wide range of applications if combined with on-off control, and may be considered for applications where little or no control of output voltage or current is necessary (e.g. LED lamps). To reach the same goal, interleaved operation of two converters is explored.

Section 2 of this paper presents a method for design of resonant converters that achieve interleaved and self-oscillating operation via passive interconnection network. Section 3 presents experimental results of an interleaved resonant boost DC/DC converter operating at over 110 MHz. Finally, section 4 concludes the paper.

2. Self-Oscillating Self-Interleaved Topology

A general schematic of the proposed method is shown in Figure 1. The system is composed of a pair of class E inverters, class E rectifiers and a passive interconnection between inverter stages. The

switching device considered in this paper is a MOSFET. The proposed technique is applicable for all class E derived converters.

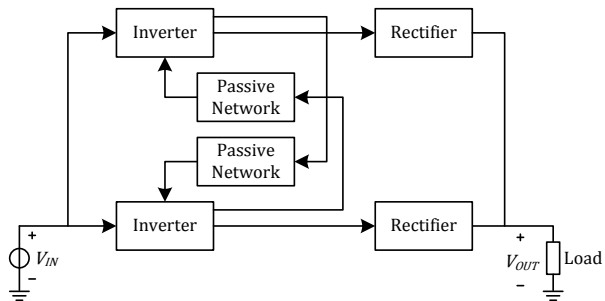


Fig. 1. A general overview of the presented topology. Interleaved converter is composed of two inverters, two rectifiers, and a passive interconnection between the inverter stages.

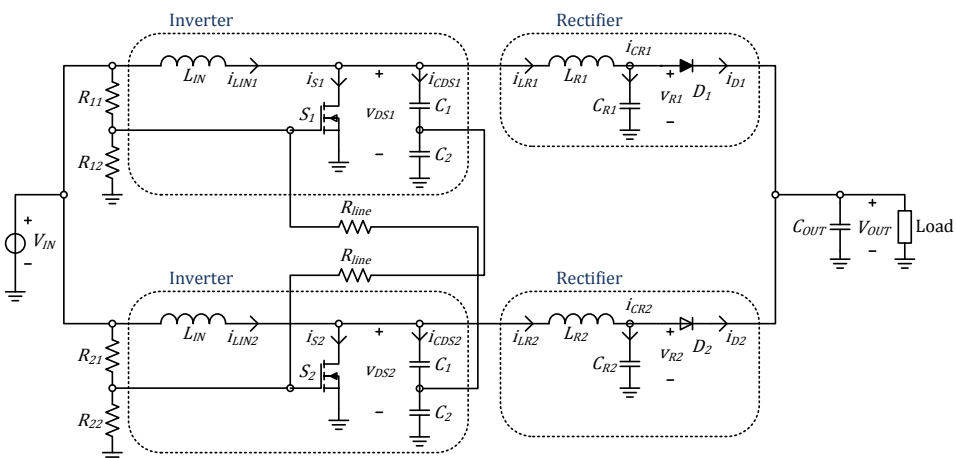
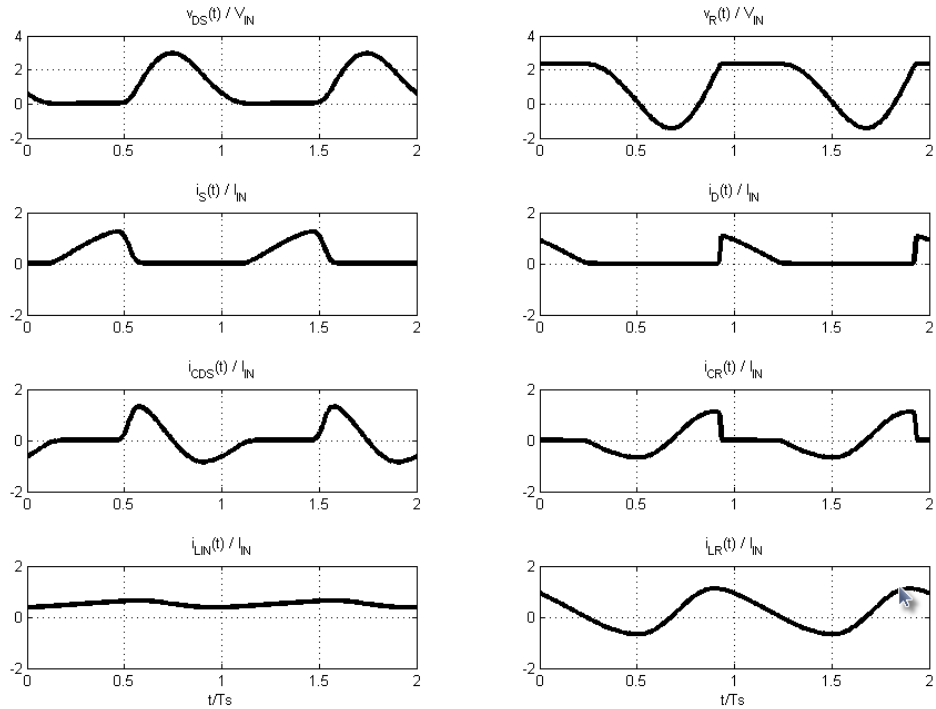


Fig. 2. Schematic of interleaved, self-oscillating class E derived resonant boost converter.

2. 1. Interleaved Topology Analysis

Implementation of the proposed method with two resonant boost converters is shown in Figure 2. This topology was chosen for verification of the method due to its small component count, and small input inductance which is part of the resonant network. This is beneficial in terms of converter size reduction and shorter transient response time, but is not critical for operation of the converter. Analysis and design procedure of the resonant boost converter are described by Redl et al. (1989) and Burkhart et al. (2010). In figure 3, simulated waveforms of the interleaved converter are presented.



(a) (b)

Fig. 3. Important voltage and current waveforms of the inverter (a) and the rectifier (b) stage of the resonant boost converter in self-oscillating interleaved mode of operation. Voltage and current waveforms are normalized to input voltage V_{IN} and average input current I_{IN}, respectively. Time axis is normalized with the converter switching period.

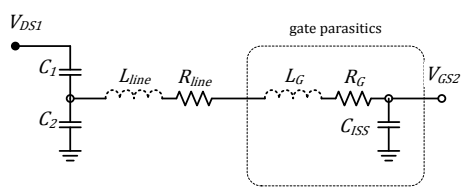


Fig. 4. Topology of the interconnection network. Capacitors C_1 and C_2 form a voltage divider for the drain voltage V_{DS1}, which is to be delivered to the gate of the switch S_2. R_{line}, R_G and C_{ISS} provide time delay in the signal path in order to achieve zero voltage switching (ZVS). L_{line} and L_G are not desired in the interconnection network but are likely to be present.

Apart from their conventional role, each inverter stage acts also as a gate driver for the switch in the opposing inverter stage. Due to circuit symmetry, without loss of generality we may concentrate on effect

of drain voltage V_{DS1} of S_1 on the gate of S_2. V_{DS1} is delivered through the interconnection network (figure 4) to the gate of S_2. The interconnection network provides necessary amplitude level transformation and the phase shift adjustment between drain and gate voltages, and also contributes to the resonant tank, as explained later. Rectifiers transform outputs of the inverters into DC output voltage V_{OUT}.

The DC bias for $V_{GS1,2}$ is provided via resistive voltage dividers $R_{11} - R_{12}$ and $R_{21} - R_{22}$, respectively. The resistance ratio is the same for both dividers. In order to ensure proper start of oscillations, the DC bias should be slightly above the switch threshold voltage. It is also beneficial if slightly different resistance values are chosen so there are different time constants for S_1 and S_2. Note that the DC bias in this configuration is directly scaled with V_{IN}. This may not be desirable in some designs; however it is chosen in this case due to simplicity and because it is not critical for the demonstration of converter operation. From figure 3 it may be observed that switch duty cycle is slightly lower than 50%. V_{GS} is a scaled-down version of V_{DS}; in case of 50% of duty cycle V_{GS} would not contain enough "width" unless ZVS restriction is lifted, which is not desirable efficiency-wise. In order to maintain ZVS condition, the default operation of the converter implies the switch duty cycle lower than 50%.

The operating frequency is strongly dependent on the values of the resonant elements, the input and output voltage of the converter and the duty cycles of the switching components. The exact dependency in case of resonant boost converters is not provided in this paper and is subject of future research. Few observations may aid in converter design, however. To simplify the analysis, large input inductance is assumed (indeed, large L_N may be selected for the design), as well as sinusoidal output current of the inverter and the switch duty cycle of 50%. Under these assumptions, inverter and rectifier stages may be designed separately. For more information, the reader is referenced to papers of Redl et al. (1989), Ivaşcu et al. (1992), Andersen et al. (2011), and Kazimierczuk et al. (2005). Due to circuit symmetry, phase shift between V_{DS1} and V_{DS2} is 180° regardless of operating frequency. However, according to the paper provided by Kazimierczuk et al. (2005), the phase shift between fundamentals of V_{DS} and V_{GS} of the same transistor should be 196° in order to achieve ZVS (zero voltage switching) and ZdVS (zero voltage derivative switching) conditions. To provide additional phase shift of 16°, the interconnection network is to be designed accordingly. The transfer function of the resonant network is given by

$$H_{D1G2}(j\omega) = \frac{C_1}{C_1 + C_2 + C_{ISS}} \frac{1}{1 + j\omega C_{ISS}\left(\frac{C_1 + C_2}{C_1 + C_2 + C_{ISS}}\right) R_N} \tag{1}$$

where C_{ISS} is the total input capacitance of the MOSFET device; C_1 and C_2 form a capacitive divider. The total network resistance R_N and inductance L_N are defined as

$$R_N = R_{line} + R_G \tag{2}$$

$$L_N = L_{line} + L_G \tag{3}$$

Note that network inductance L_N is omitted from (1). In general, L_N is not desired in the feedback path as it can form a parasitic resonance with the capacitances in the interconnection network; therefore, the circuit layout should be designed in such a way to minimize it.

To give an impression on the typical values of the network components, an example design of the interconnection network is provided. Let us assume that V_{DS}/V_{GS} ratio of 10 is required and that the operating frequency f_S is 100 MHz. Essentially, $H_{D1G2}(j\omega)$ is a low-pass *RC* filter with attenuation of $C_1/(C_1 + C_2 + C_{ISS})$. C_{ISS} is determined by choice of the switching device; C_1 and C_2 are determined by the desired value of the total drain-source capacitance C_{DS}. If we assume that R_N is small compared to impedance of C_{ISS}, then the values of C_1 and C_2 are determined from the following equations:

$$\frac{C_1}{C_1 + C_2 + C_{ISS}} = \frac{V_{DS}}{V_{GS}} \tag{4}$$

$$\frac{C_1\,(C_2 + C_{ISS})}{C_1 + C_2 + C_{ISS}} = C_{DS} - C_{OSS} \tag{5}$$

where C_{OSS} is the total output capacitance of the switch. R_N is then determined from (1) to provide the required phase shift. A small error in the final result; the voltage ratio is slightly larger than desired.

Note that V_{DS} voltage waveform of the inverter stage is scaled up linearly with V_{IN}; and so is V_{GS}. This is a fundamental limitation of this method. If employed MOSFET device does not have any protection circuitry to limit V_{GS}, the device failure may occur. In order to optimize the design according to the switch voltage limitations, the maximum allowed V_{GS} should be achieved at the maximum allowed V_{DS}.

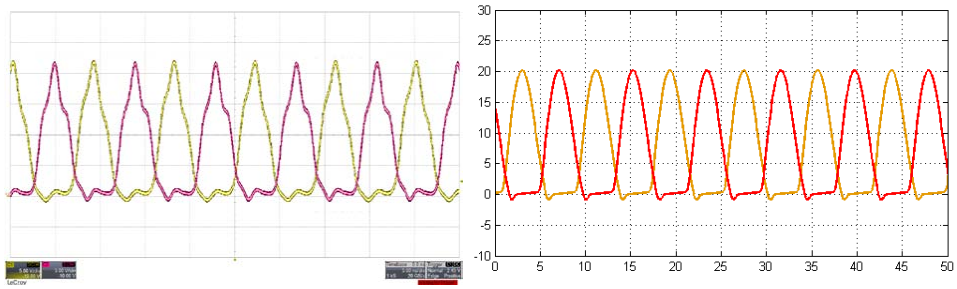
Due to interleaved operation, electromagnetic interference at switching frequency and odd harmonics is expected to be reduced compared to single phase counterpart for the same power level. In VHF designs, however, it may be difficult to achieve very high noise rejection using this technique as a mismatch in such circuit would certainly appear. Nevertheless, this property is appealing since the largest amount of energy in the circuit is carried by the first harmonic.

3. Experimental Results and Evaluation

A prototype converter was built and evaluated in practice in order to verify the presented principle. Component values from simulations were chosen for the final design and are provided in table 1. Additionally, small adjustments were made in the simulation to the given values, in order to take some parasitic effects into account. Most notably, parasitic capacitances of the MOSFET and the diode devices were added (the values extracted from the datasheets); L_{IN} and L_R were slightly increased due to parasitic inductances of the layout.

Table 1. Components used in the 110 MHz prototype converter design

switch pair $S_1 - S_2$	BLF645, dual RF LDMOS
input inductance L_{IN}	68nH
capacitance pair $C_1 - C_2$	70 pF / 200 pF
rectifier diodes	MSS1P3, Schottky
rectifier inductance L_R	22 nH
rectifier capacitance C_R	68 pF
interconnection network resistance R_{line}	6.5 Ω
resistance pair $R_{11} - R_{12}$	19.5 kΩ / 3.9 kΩ
resistance pair $R_{21} - R_{22}$	21.5 kΩ / 4.3 kΩ



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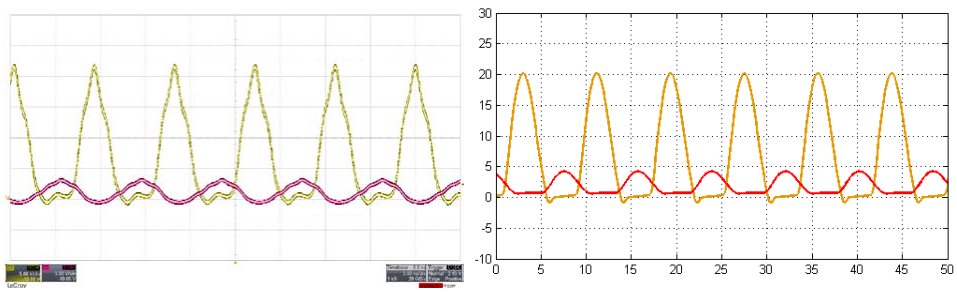

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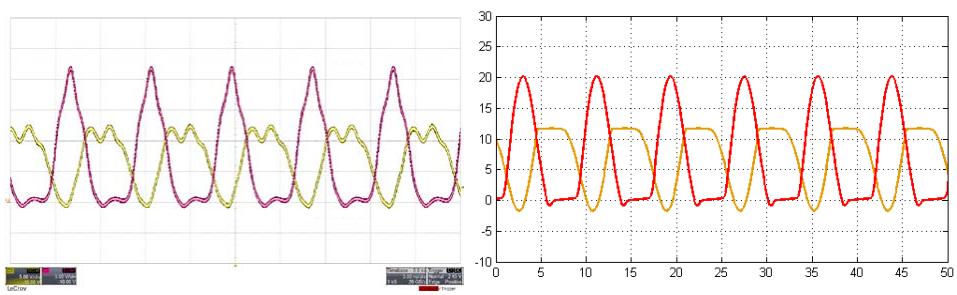

c)

Fig. 5. Measured (left) and corresponding simulated (right) results of the prototype converter. Figure (a) shows voltages V_{DS1} and V_{DS2} (yellow, red), figure (b) voltages V_{DS1} and V_{GS1} (yellow, red), and figure (c) voltage V_{R1} and V_{DS1} (yellow, red). Voltage and time resolutions for all figures are 5 V/div and 5 ns/div, respectively.

Measured waveforms are presented in figure 5 and were obtained under following conditions: $V_{IN} = 7$ V, $I_{OUT} = 400$ mA, and $V_{OUT} = 11$ V. The achieved switching frequency was 110 MHz. In general, waveforms correspond well to simulation results; major differences are due to effects of the oscilloscope probe bandwidth limitations, as well as the presence of parasitic inductances of the component packages which were not accounted for in the simulation. The reader is referred to the report by Andersen et al. (2011) for more insight. Parasitic resonance at higher frequency may be observed in the waveforms as some parasitics were not considered or were partially considered in simulations. A slight difference was

observed in the waveforms due to non-ideal symmetry in the circuit. Switching frequency is also lower than expected from simulations due to parasitic inductances, but also due to capacitance of the oscilloscope probe. Figure 6 shows efficiency of the converter versus output power P_{OUT} for fixed output currents of 0.4 A and 0.5 A. Increase of P_{OUT} is achieved by increasing V_{IN} from 6 V to 9V in steps of 0.5 V. The apparent drop in efficiency with increase of P_{OUT} is primarily due to conduction losses in the rectifier stages; R_{line} also contributes to overall losses in the circuit. Note that further increase of the output current is possible, but in case of low input voltage the duty cycle of the rectifier diodes becomes 1 and the rectifiers seize to operate as intended.

Note that no control technique of the output voltage or output current was implemented; this issue is to be addressed as part of ongoing research. An on-off control technique already demonstrated (Rivas et al., 2006, Pilawa-Podgurski et. al., 2009, Burkhart et. al., 2011.) is considered as a good candidate.

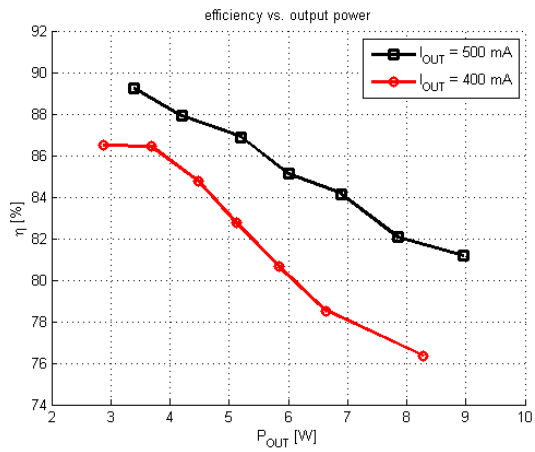

Fig. 6. Efficiency vs. output power at fixed output currents of 0.5 A (black) and 0.4 A (red).

4. Conclusion

A technique for design of self-oscillating class E based resonant converters has been presented. Interleaved operation and simplified gate driving are achieved simultaneously with very small number of additional passive components.

Due to interleaved operation and resonant operation of the converter, EMI interference is expected to be reduced compared to a single phase converter if high level of symmetry is achieved; as a part of the future research, this claim is to be addressed in more detail. Both ZVS and ZdVS operation at switch turn on are possible which is verified through simulations; a detailed design procedure for achieving this is to be determined.

The proposed technique is validated experimentally on a pair of resonant boost converters, which operate at switching frequency of above 110 MHz. Measured results are presented and are in good agreement with theoretical and simulation results. The major differences between theoretical expectations and implementation are due to parasitic inductances of the component packages and layout. It is our conclusion that the proposed method may lead to effective converter design at VHF frequencies.

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Appendix D

Very High Frequency Interleaved Self-Oscillating Resonant SEPIC Converter

IEEE European Conference on Power Electronics and Applications (EPE ECCE Europe 2013, France)

Very High Frequency Interleaved Self-Oscillating Resonant SEPIC Converter

Milovan Kovacevic, Arnold Knott, Michael A. E. Andersen
Technical University of Denmark
Ørsteds Plads, Building 349
2800 Kgs. Lyngby, Denmark
Phone: +45 / 4525 5639
Fax: +45 / 4588 0117
Email: {mikov, akn, ma}@elektro.dtu.dk
URL: http://www.elektro.dtu.dk

Keywords

«very high frequency power converter», «resonant converter», «zero voltage switching», «interleaved converters», «self-oscillating»

Abstract

This paper describes analysis and design procedure of an interleaved, self-oscillating resonant SEPIC converter, suitable for operation at very high frequencies (VHF) ranging from 30 MHz to 300 MHz. The presented circuit consists of two resonant SEPIC DC-DC converters, and a capacitive interconnection network between the switches which provides self-oscillating and interleaved operation. A design approach to ensure zero voltage switching (ZVS) condition of the MOSFET devices is provided.
To verify the proposed method, an 11 W, 50 MHz prototype was built using low-cost VDMOS devices and experimental results are presented. Peak achieved efficiency was 87%.

Introduction

A constant drive for miniaturization of power converters inevitably leads to increase of converter switching frequency. Reactive components scale down in both physical size and value, which permits use of power converters in applications with severe size constraints. This is especially beneficial regarding magnetic components, as they are typically the biggest contributors to the size of power converters. Inductance values required for operation at very high frequencies could easily be achieved with air core inductors, eliminating core loss entirely. For operation above 30 MHz, requirements for EMI filtering are significantly relaxed: EMI filters could be reduced to a few SMD components, or removed completely from a design. For some applications, for example LED drives, it is also beneficial if the power converter does not require electrolytic capacitors for voltage/current filtering, as they might limit the lifetime of LED lamps.

High switching frequencies impose new design challenges as well. With exception of very low power and voltage levels, hard-switched converters are unsuitable for operation at frequencies above a few MHz due to prohibitively large switching losses [1]. Generating signals for high-side switches is very difficult [2], which further limits topology selection, except in low-voltage converters [3]. Losses are further increased if hard gating is employed, which is exclusively the case for commercial DC-DC converters today.

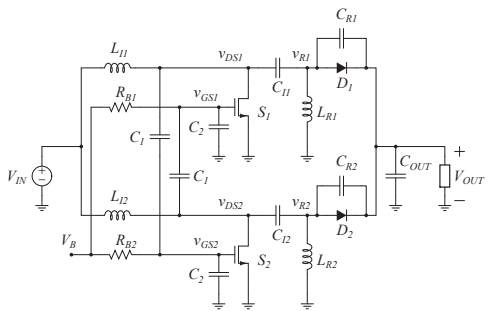


Fig. 1: Schematic of the interleaved, self-oscillating resonant SEPIC converter.

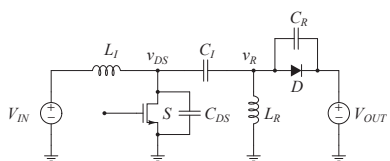


Fig. 2: Resonant SEPIC converter topology.

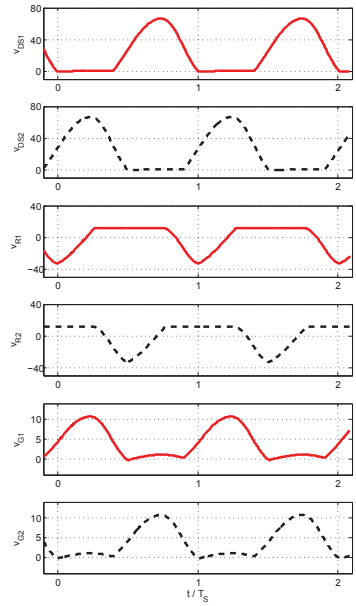


Fig. 3: Simulated waveforms of the drain, rectifier, and gate voltages of the interleaved self-oscillating resonant SEPIC converter; $V_{IN} = 24$ V and $V_{OUT} = 12$ V.

To work around these problems, resonant converter topologies need to be considered in order to minimize or eliminate some of the switching loss mechanisms. Resonant [4–6] or multiresonant [1, 7] gate driving techniques need to be employed as well, thereby reducing the gating loss by recovering portion of the energy from the gate capacitances. Since there are no gate driver solutions intended for operation above 30 MHz currently available on the market, gate drivers for VHF converters are typically developed using discrete components.

This paper presents a recently developed technique to achieve interleaved, self-oscillating operation of two resonant converters, suitable for power conversion at frequencies in VHF (30 MHz - 300 MHz) range, and a design procedure for a step-down resonant SEPIC converter utilizing aforementioned technique. A general structure of the proposed converter, as well as the interconnection network which provides self-oscillating behavior and interleaved operation, are described. Design procedure for the proposed converter is provided. Finally, experimental results of an 11 W, 50 MHz prototype are presented.

Proposed Converter

Fig. 1 shows the proposed converter topology. Two resonant SEPIC converters [7], as shown in Fig. 2, are coupled via capacitive interconnection network, which provides gate signal generation for driving the MOSFET devices. The circuit is symmetrical, and the gate voltages are in phase with the drain voltages of opposing MOSFETs due to capacitive voltage dividers; thus providing interleaved operation. Typical voltage waveforms of the interleaved resonant SEPIC converter are shown in Fig. 3.

This section is organized as follows:

- topology and properties of the resonant SEPIC converter
- the interleaved converter topology
- the interconnection gate drive network
- converter startup

Resonant SEPIC Converter

Compared to the class E converter [4, 8], which has bulky input and output inductances, in resonant SEPIC converter topology all reactive components are part of the resonant tank and therefore are small in value. Furthermore, fewer inductors are necessary, as well as lower component count in general [**?**]. This is particularly important if we have in mind that at RF frequencies inductors typically have low Q factors due to skin and proximity effects, which increase conduction losses.

Due to presence of 5 resonant elements and 2 switching devices, even with ideal components the circuit in Fig. 2 is very difficult to describe analytically [7]. The situation is complicated even further due to nonlinearity of the parasitic capacitances of the semiconductor devices. To accurately predict the behavior of the circuit, a simulation program and precise component models are required.

It was observed that not all reactive elements are necessary for the correct circuit operation, although they will certainly appear in a physical prototype. The absolute minimum requirements are two inductors and two capacitors, either C_{DS} and C_I, or C_R and C_I. In Fig. 4 the 4-element resonant network seen from the drain terminal is shown, as well as two 3-element simplified networks; note that L_I is excluded since it remains the same in all three configurations. With the appropriate components choice, these networks may have exactly the same input impedance at all frequencies, which is the impedance seen by the drain terminals of the MOSFETs. Therefore, in the design process of the proposed interleaved converter, one of the 3-element networks can be used instead, thus reducing the number of unknowns in the design by one. The transformation between the networks in Fig. 4 is given in Table I. Capacitances and inductances are normalized with respect to $C_{I,1}$ and $L_{R,1}$. n and k are the capacitance ratios $C_{DS,1}/C_{I,1}$ and $C_{DS}/C_{I,1}$, respectively. Note that k must always be less than or equal to n. This transformation affects the output impedance of the network, which means that the output voltage and current have to be scaled as well in order to obtain identical circuit behavior. For example, if the 3-element network 1 is transformed into the 3-element network 2, output impedance is scaled down by a factor of $(1+n)^2$; equivalently, the output current is increased $1+n$ times, and the output voltage is decreased by the same factor.

Interleaved Resonant SEPIC Converter

In the case of the proposed converter from Fig. 1, it was found that the resonant/switching frequency may be approximately determined from:

$$f_S \approx \frac{1}{2\pi\sqrt{L_I(C_I + C_{DS,eq})}} \tag{1}$$

Capacitance $C_{DS,eq}$ is defined as the equivalent drain to source capacitance:

$$C_{DS,eq} = C_{OSS} + \frac{C_1(C_2 + C_{ISS})}{C_1 + C_2 + C_{ISS}} \tag{2}$$

The exact value of f_S also depends on duty cycle of the switch and the diode, which are not easy to predict - especially if nonlinear capacitances of the semiconductor components are taken into account. Nonetheless, equation (1) is a good starting point for the design procedure; reactive elements could be scaled up or down in order to adjust for desired output power or frequency. For example, increase in circuit capacitances N times would result with a converter with $\sqrt{N}$ lower switching frequency and $\sqrt{N}$ higher power output. If capacitances are scaled up and inductances are scaled down by the same factor,

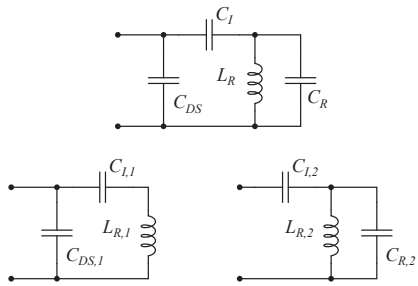


Fig. 4: Resonant network seen by the drain terminal of the MOSFETs, with the exclusion of the input inductor L_I; original (top) and two alternatives (bottom). The components of these networks may be chosen in such a way that all three circuits have the same input impedance.

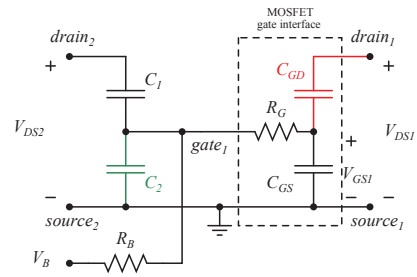


Fig. 5: A part of the interconnection network used with the resonant SEPIC converter to obtain the self-oscillating and interleaved operation. Voltage divider formed by C_1, C_{GS}, and C_2 (optional), determines the amplitude of the gate voltage. Note the parasitic feedback from the drain of the same MOSFET. Bias voltage for the gate terminal is provided through resistor R_B.

Table I: Network transformations.

	C_I	C_{DS}	C_R	L_I
original	$(1+n-k)\,C$	$k\,C$	$(1+n-k)\,(n-k)\,C$	$L/(1+n-k)^2$
alternative (1)	C	$n\,C$	—	L
alternative (2)	$(1+n)\,C$	—	$n\,(1+n)\,C$	$L/(1+n)^2$

the switching frequency would remain the same and the power output would increase N times.

As it was observed in [7], the waveforms do not deviate significantly with change of voltage transformation ratio M, and this also holds true for the interleaved self-oscillating SEPIC converter. This property is very useful, since it allows easy change of specifications with only minor adjustments to the converter components.

Interconnection Network

Several gate drive techniques are described in the literature, and in that sense RF DC-DC converters may be separated into two major groups: oscillator-driven [1, 2, 5, 7] and self-oscillating converters [4, 6].

The interconnection network from the drain of S_2 to the gate of S_1 is shown in Fig. 5. C_1 and C_2, together with the gate capacitance of the MOSFET C_{GS}, form a capacitive voltage divider, thus generating the signal for driving the other switch.
Gate resistors R_{B1} and R_{B2} provide biasing for the MOSFET gates. During the converter startup, R_{B1} and R_{B2} form $R-C$ time constants with the gate capacitances of S_1 and S_2. In order to reduce the startup time, these time constants should be different, or alternatively, independent bias voltages should be used.

If resistance R_G is small compared to impedance of the MOSFET input capacitance C_{ISS} (which is usually the case), then the gate voltage v_{GS} is approximately given as:

$$v_{GS}(t) = \frac{C_1}{C_1+C_2+C_{GD}+C_{GS}}\,v_{DS,AC}(t) + \frac{C_{GD}}{C_1+C_2+C_{GD}+C_{GS}}\,v_{DS,AC}(t) + V_B \tag{3}$$

The first term in (3) represents feedback from the drain voltage of the opposing MOSFET. The second term is due to parasitic capacitance C_{GD} and is undesirable. The operation point of the switch in the OFF-state might shift into the saturation region and produce significant losses, which also shortens the switch lifetime or, in more severe cases, the switching device may be destroyed. Therefore, it is recommended to use switches with small C_{GD} capacitance in the design, and the feedback network needs to provide enough gain in the primary feedback. This is done by appropriate sizing of C_1 and C_2. Additional benefit of having nonzero C_2 in the circuit which helps suppressing parasitic high frequency oscillations on the gate, which may appear due to stray inductances in the circuit. However, increase of C_1 and C_2 is limited by ZVS condition. C_I needs to be at least two times larger than $C_{DS,eq}$ in order to achieve ZVS operation.

There are some drawbacks to this technique. In order to obtain circuit symmetry at VHF frequencies, layout needs to be symmetrical and the circuit components should have low tolerances. Since there is a purely capacitive signal path from drain to gate terminals, any parasitic inductance in the circuit might introduce ringing in the gate voltage waveforms. As well as in [6], this self-oscillating scheme shows lower dependency of output power with the bias voltage compared to [9]. Therefore it is reasonable to consider burst-mode control scheme [1, 5, 7, 10] for the proposed converter, which is a subject of further research.

Converter Startup

Start-up of the circuit is achieved by setting the gate bias voltage slightly above the MOSFET threshold voltage, so the switching devices enter saturation mode. A simplified AC equivalent of the inverter side is shown in Fig. 6. The MOSFETs are modeled as voltage controlled current sources.

The loop formed by the MOSFETs and the capacitive voltage dividers is unstable; hence, amplitudes of the drain (and consequently, gate) voltages increase. This increase is bounded by the fact that the MOSFETs eventually start entering the ohmic region, thus limiting the effective gain in the loop. In the steady state, the MOSFETs do not enter saturation region.

Typical startup gate and drain waveforms are shown in Fig. 7, as a response to a step change in V_B at $t = 0.2$ µs. Until the oscillations start, the response of the gate voltages is described completely by time constant τ_G defined as

$$\tau_G = R_B(C_{ISS} + C_{DG} + C_1 + C_2) \tag{4}$$

and ends when the MOSFETs enter saturation. For the circuit in Fig. 6 to be unstable, the following condition has to be satisfied:

$$g_m \, Q \, Z_0 > \frac{1}{x} \tag{5}$$

where Q is the Q-factor of the resonant tank, Z_0 is the reactance of the inductors/capacitors at the resonant frequency, g_m is the MOSFET transconductance, and x is the scaling factor of the capacitive voltage divider in (3). For a given switching frequency and power level, g_m, Q, and Z_0 should be maximized in order to minimize the transient time.

Design Procedure

A method was proposed in [7] which relies on separate design of the inverter and rectifier stages. However, that procedure has been found unsuitable for the self-oscillating interleaved converter design. As it was discussed in the previous section, it is very difficult to determine the switching frequency a priori due to complexity of circuit operation. More importantly, it is not guaranteed that a converter designed to operate at a certain frequency might not operate at that particular frequency when used in the interleaved

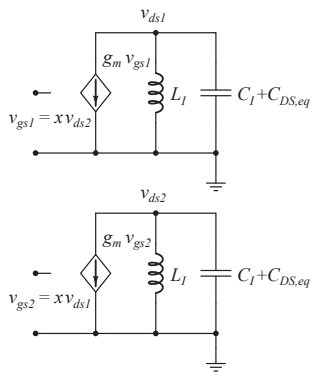


Fig. 6: Simplified AC equivalent circuit of the inverter stages during startup process. The MOSFETs, while in saturation, are modeled as voltage controlled current sources.

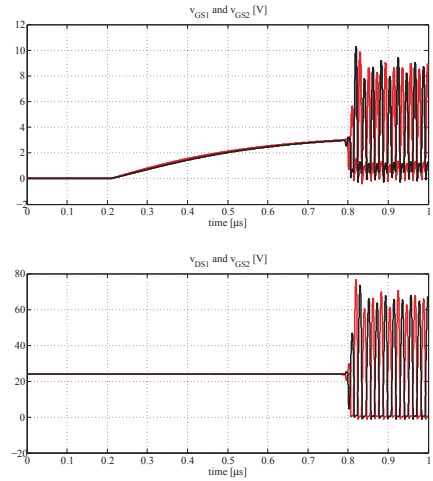


Fig. 7: Gate (top) and drain (bottom) waveforms during the converter startup.

design. Therefore, a direct synthesis method is proposed in this section.

The design procedure starts from specifications for output power P_{OUT}, switching frequency f_S, and input voltage V_{IN}. Required component values will be finally determined from the output power P_{OUT} specification by scaling of the reactive components. At this stage of the design process, initial values for C_R and L_R are $C_R = 0$ and $L_R = 1.5L_I$.

Capacitance C_1 is directly determined from (3):

$$C_1 = (C_2 + C_{GS} + C_{GD}) \frac{V_{GS,max}}{V_{DS,max} - V_{GS,max}} \tag{6}$$

where C_2 may be chosen arbitrarily as long as it does not yield high capacitance value for C_1. For low voltage applications or when the C_{GS} is large, C_2 may be omitted. The ratio between the SEPIC "flying" capacitance C_I and equivalent drain to source capacitance $C_{DS,eq}$ is a limiting factor for ZVS operation; a good initial value for C_I was found to be at least 2-3 $C_{DS,eq}$. The transformation provided in Table I should be applied to include C_R in the final design. After C_I is selected, input inductance L_I is determined from (1):

$$L_I = \frac{1}{(2\pi f_S)^2} \frac{1}{C_I + C_{DS,eq}} \tag{7}$$

Inductor L_R is then adjusted as necessary to reach ZVS operation. Impedance scaling is then applied to obtain desired frequency and output power.

The peak drain voltage $V_{DS,max}$ is expected to be around 3 times higher compared to V_{IN}. Therefore, the MOSFET has to be chosen with a voltage rating higher than $V_{DS,max}$.

Nonlinearities of the parasitic capacitances may influence the final result, and for that reason accurate modeling is beneficial. Nevertheless, even with the simple models of the transistors and diodes reasonable accuracy is obtainable.

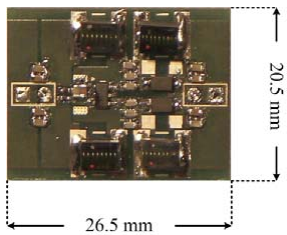


Fig. 8: Experimental DC-DC converter.

Table II: Converter component values.

Component	Value
L_I	Coilcraft air-core 82 nH
L_R	Coilcraft air-core 120 nH
C_1	C0G 13 pF
C_2	-
C_I	C0G 80 pF
$C_{S,EXT}$	-
C_{IN}	C0G 8 uF
C_{OUT}	C0G 8 uF
S	Fairchild FDC8602
D	NXP PMEG6010

Experimental Results

Experimental setup was built to verify the proposed design procedure (see Fig. 8). The DC-DC converter specifications are as follows:

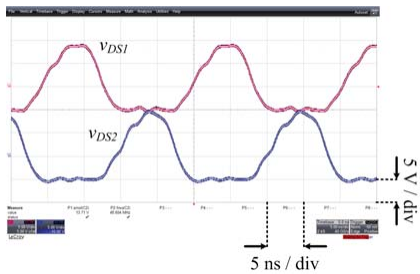
- input voltage $V_{IN} = 24$ V
- output voltage $V_{OUT} = 11$ V
- output current $I_{OUT} = 1$ A
- switching frequency $f_S = 50$ MHz

A complete list of components used is presented in Table II.

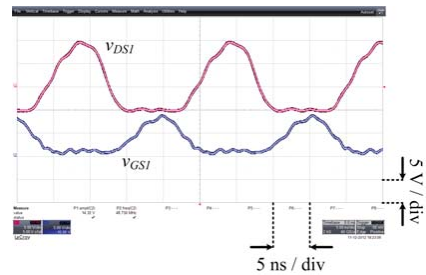
The MOSFET device to be used in the design needs to be able to withstand at least 3 times the input voltage. Therefore, 100 V rated devices were considered, and FDC8602 dual MOSFET from Fairchild Semiconductor was chosen since it offered a good balance between $R_{DS,on}$ and parasitic capacitances C_{ISS} and C_{OSS}. On the other hand, the downsides are the presence of the stray inductance and high thermal resistance of the package. Experimental voltage waveforms of the designed converter are provided in Fig. 9. Note the high-frequency ringing due to finitely small inductances of the component packages and PCB traces.

The circuit shows little tolerance to non-symmetry, therefore direct measurements with a 9.5 pF oscilloscope probe would disturb the operation of the converter, especially of v_D and v_R nodes. The measurements of these nodes were obtained through 2.7 pF capacitance instead (see Fig. 10), which gives the scaling factor of 0.22 and removes the DC component from the waveform. With input voltage of 24 V, expected peak voltage across the MOSFETs should be around 72 V. In Fig. 9a, peak-to-peak v_{DS} voltages are 15 V. This gives $V_{DS,max}$ of 68 V which matches well with expectations.

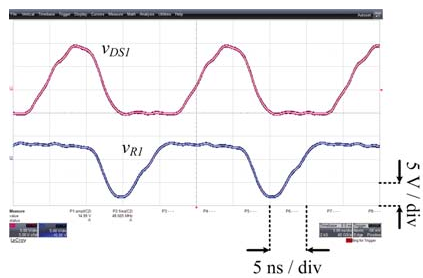
v_{GS} was designed to have 10 V peak-to-peak value. In Fig. 9b the direct measurement is provided, and it can be observed that the amplitude is close to 8 V, indicating the influence of the probe capacitance. Measured switching frequency was 48.7 MHz when the probe was connected to the board via 2.7 pF capacitor. The frequency is 5 % off the target value, which is accredited mainly to the simplicity of the model and equation (1).



(a) Drain voltages $v_{DS1}(t)$ and $v_{DS2}(t)$



(b) Drain and gate voltages $v_{DS1}(t)$ and $v_{GS1}(t)$



(c) Drain and rectifier voltages $v_{DS1}(t)$ and $v_{R1}(t)$

Fig. 9: Experimental waveforms of the prototype converter.

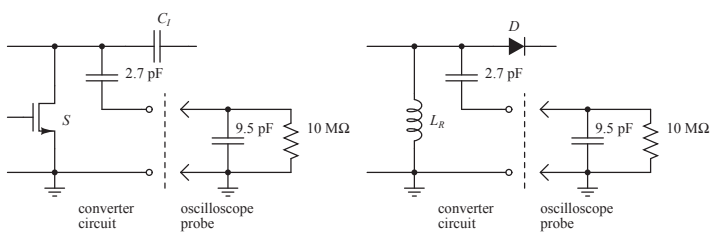


Fig. 10: Measurement setup for drain (left) and rectifier (right) voltages.

Conclusion and Future Work

This paper presents a gate driving scheme which provides self-oscillating and interleaved operation of two resonant SEPIC converters. The only components of the gate drive which do not belong to the converter topology are two capacitors and two biasing resistors. These components are typically small in size, which makes this gate drive method very component and space efficient. A design procedure for the interleaved SEPIC converter has been proposed, and experimental results have verified its effectiveness. A 50-MHz, 11 W converter has been designed and implemented, using only low-cost diodes and VDMOS switches. The peak achieved efficiency was 87%.

The circuit layout needs to be as symmetrical as possible in order to achieve optimal operation. Output power is not significantly influenced by variation of the gate bias voltage. As part of the ongoing re-

search, implementation of the burst-mode control with this gate driving technique will be investigated, for which this gate drive technique shows promising results.

As this paper has demonstrated, it is possible to obtain acceptable efficiency, small converter size, and low cost in VHF power conversion.

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Appendix E

A VHF Interleaved Self-Oscillating Resonant SEPIC Converter with Phase-Shift Burst-Mode Control

IEEE Applied Power Electronics Conference and Exposition (APEC 2014, TX, USA)

A VHF Interleaved Self-Oscillating Resonant SEPIC Converter with Phase-Shift Burst-Mode Control

Milovan Kovacevic, Arnold Knott, Michael A. E. Andersen
Department of Electrical Engineering
Technical University of Denmark
Kgs. Lyngby, Denmark
Email: {mikov, akn, ma}@elektro.dtu.dk

***Abstract*—This paper presents design and implementation of the phase-shift burst-mode control method for interleaved self-oscillating resonant SEPIC converters for LED lighting applications. The proposed control method utilizes delays in the turn-on and turn-off of the power stage and control circuitry in order to reduce requirements for the comparator in the regulation circuit. The control method is experimentally evaluated on a 49 MHz dc-dc converter prototype, and the results are presented. The designed converter demonstrates peak efficiency of 81%, maintains efficiency above 75% from 20% load to full load, and is implemented using low-cost switches and integrated circuits.**

I. Introduction

Reducing the physical size of electronic equipment in power applications is desired in order to add more features into existing products, integrate power converters in places normally unfit for such equipment, and reduce system cost. Increasing the operating frequency of the converter is a direct way of reducing the size of energy storage elements such as bulky capacitors and inductors, which usually dominate the overall converter volume. Due to reduction in energy storage requirements the transient response is dramatically increased. LED lighting applications and point-of-load (PoL) converters particularly benefit from very high frequency (VHF) converters due to size, price, and weight reduction, and faster transient response.

In recent publications it has been demonstrated that VHF converters with efficiencies exceeding 80% can be implemented [1]–[18]. Due to their superior performance in terms of transient response, the most common choice of control strategy is burst mode control [1]–[4], [7], [13], [14]. This approach allows the converter designer to optimize resonant converters for operation in one operating point, and turn them on or off as necessary to maintain constant output voltage or current. The downside is that the EMI performance is the same or worse compared to a hard-switched converter at the same modulation frequency. There are only a few exceptions which utilize voltage-controlled oscillators [10] in order to improve EMI performance.

Burst-mode control implementations encountered in recent papers were either hysteresis-based [1]–[4], [7], or PWM-based with constant switching frequency [14], [19]. Hysteresis-based control tight output regulation, but it requires a high-cost, high-performance comparator with very small propagation delays.

In this paper, a phase-shift based burst mode control implementation is analyzed and experimentally evaluated, which utilizes propagation delays in the comparator, filtering elements and the power stage. The target application is highly cost-sensitive due to high production volume (dimmable LED lighting), the prototype was built using low-cost switches, diodes and ICs. Section II briefly describes the power stage. Section III provides analysis of the proposed burst-mode control method. Experimental results of the prototype are shown in section IV, and design considerations are discussed in section V. Finally, section VI summarizes achieved results and concludes the paper.

II. Power Stage

Fig. 1 presents a block diagram of the of the proposed converter. The converter consists of a VHF power stage, control circuit with the on/off output, and a signal conditioning network $H(s)$.

The power stage is implemented as an interleaved self-oscillating resonant SEPIC converter [17], where two power stages drive each other via capacitive coupling (C_{X1} and C_{X2}) between the switches S_1 and S_2 and operate in interleaved mode. The power stages are identical, eg.

$$\begin{aligned} L_{I1} &= L_{I2} = L_I \\ C_{I1} &= C_{I2} = C_I \\ C_{X1} &= C_{X2} = C_X \\ C_{S1} &= C_{S2} = C_S \end{aligned} \tag{1}$$

Schematic of the power stage is shown in Fig. 2. The most important parasitics of the semiconductor devices, diode junction capacitance and parasitic capacitances of the switches, are absorbed into the converter resonant network. Self-oscillating switching frequency f_S [17] is determined mainly by the inductance L_I and the total capacitance seen from the drain when the rectifiers are shorted, $C_{DS,tot}$

$$f_S = \frac{1}{2\,\pi\,\sqrt{L_I\,C_{DS,tot}}} \tag{2}$$

where

$$\begin{aligned} C_{DS,tot} &= C_I + C_{OSS} + C_S + C_X || C_{ISS} \\ C_{OSS} &= C_{DS} + C_{DG} \\ C_{ISS} &= C_{GS} + C_{DG} \end{aligned} \tag{3}$$

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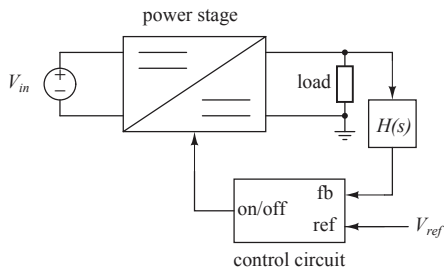


Fig. 1: Block diagram of the proposed converter.

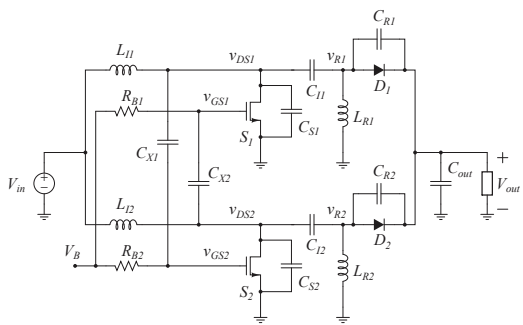


Fig. 2: Schematic of the power stage.

Oscillations start once the gate voltage becomes slightly higher than the MOSFET threshold voltage [9]. Simulated waveforms of the power stage are shown in Fig. 3. Ideally, respective waveforms of the two interleaved converters are identical and shifted by 180° out of phase.

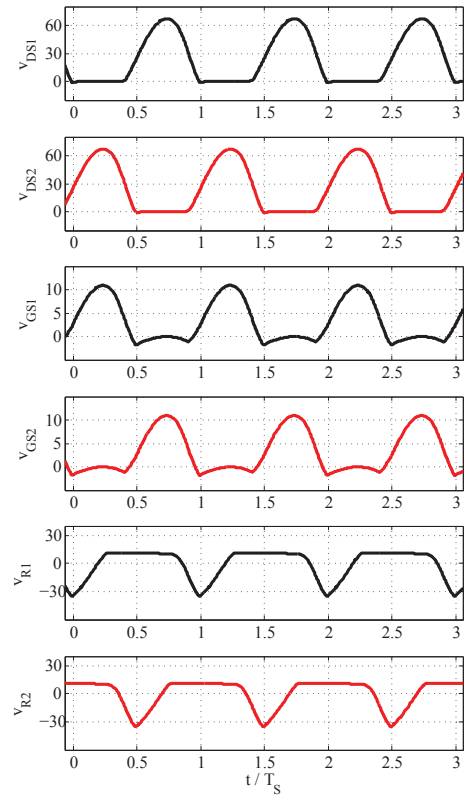


Fig. 3: Simulated waveforms of the power stage.

III. Control Strategy

If VHF ripple is neglected, the converter output can be modeled as a current source with the current value of I_0. When an on/off modulation is applied on the converter, the current delivered from the converter i_{conv} to C_{out} and the load may be approximately modeled as a current square-wave:

$$i_{conv} = \begin{cases} I_0, & \text{when the converter is ON} \\ 0, & \text{when the converter is OFF} \end{cases} \quad (4)$$

Output current I_{out} is equal to average value of i_{conv} over one modulation cycle. I_0 is not known from values of circuit components. An approximate value of I_0 can be determined from Spice simulations. Once I_0 is obtained, the output filter and the feedback circuit need to be designed to provide desired modulation frequency f_M at a specified load.

Fig. 4 shows the proposed control circuit. Feedback is taken to the comparator from the output voltage through a voltage divider / low-pass filter $H(s)$, formed by R_{FB1}, R_{FB2}, and C_{FB}. The comparator turns the switches S_{aux1} and S_{aux2} on and off, according to the voltage difference at its input. When S_{aux1} and S_{aux2} are on, v_{GS1} and v_{GS2} are zero and the oscillations are inhibited. Once S_{aux1} and S_{aux2} are off, v_{GS1} and v_{GS2} start to increase from 0 to V_B as C_{ISS1} and C_{ISS2} are charged through R_{B1} and R_{B2}. When v_{GS1} and v_{GS2} exceed the power MOSFET threshold voltage V_{th}, switches S_1 and S_2 enter saturation and initiate oscillations in the power stage. $H(s)$ has two primary purposes: to filter high frequency noise and adjust the feedback voltage level. It also contributes to propagation delay in the feedback loop.

A low-frequency model has been derived and is presented in Fig. 5. The VHF power stage is modeled as an on-off controllable DC current source. The conditioning circuit at the controller input is represented by a simple transfer function as

$$H(s) = \frac{A_{FB}}{1 + s\,\tau_{FB}} \quad (5)$$

where

$$A_{FB} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}}$$
$$\tau_{FB} = C_{FB}\,(R_{FB1} || R_{FB2}) \quad (6)$$

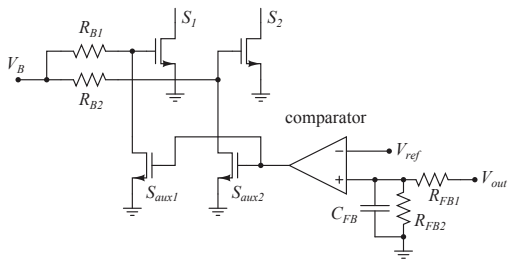


Fig. 4: Schematic of the phase-shift burst-mode controller.

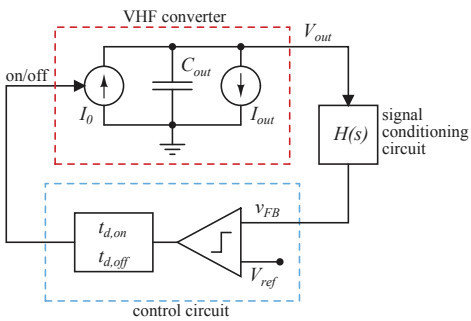


Fig. 5: The proposed circuit model.

The comparator in the control circuit model is ideal, the propagation delay of the real comparator is added into the delay block. The delay block is represented by two different time delays, since the shutdown of the power stage is significantly faster than the startup sequence. This is because shutdown is performed by the auxiliary switches S_{aux1} and S_{aux2}, while during startup C_{ISS} is passively charged from the bias voltage V_B through the biasing resistors.

In Fig. 6, characteristic voltage and current levels from a numerical example of the model are shown, where

- C_{out} = 3.3 µF
- I_0 = 1.04 A, I_{out} = 0.52 A
- R_{FB2} = 2 kΩ, R_{FB1} = 8.2 kΩ
- C_{FB} = 220 pF
- $t_{d,on}$ = 700 ns + 170 ns = 870 ns
- $t_{d,off}$ = 170 ns

The parameters are chosen to approximate the experimental setup described in section IV. $v_{gate}(t)$ represents the gate voltages of S_1 and S_2 with removed VHF component. $V_{out}(t)$ passes through the single-pole transfer function $H(s)$ and results in a distorted triangular waveform $v_{FB}(t)$. Average value of $v_{FB}(t)$ is slightly lower than the referent V_{ref} voltage, which is due to $t_{d,on} > t_{d,off}$. This is also the cause of the duty cycle of the comparator output $v_{cmp}(t)$ to be lower than 50%. Since the referent output voltage is 10 V, a small offset can be observed in $V_{out}(t)$. This offset is dependent on the duty cycle of the power stage, the time

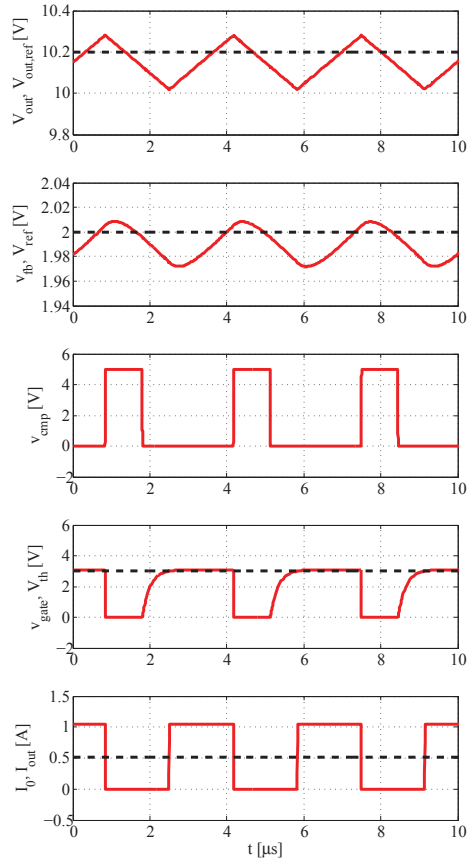
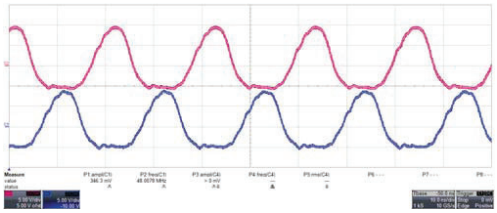


Fig. 6: Characteristic voltage and current waveforms of the model from Fig. 5.

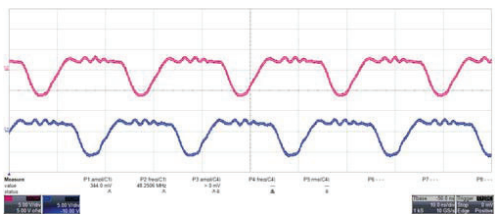
difference $t_{d,on} - t_{d,off}$, and C_{out}. $t_{d,on}$ depends on the voltage difference between V_B and V_{th}. Obtained modulation frequency is very close to 300 kHz.

IV. Experimental Results

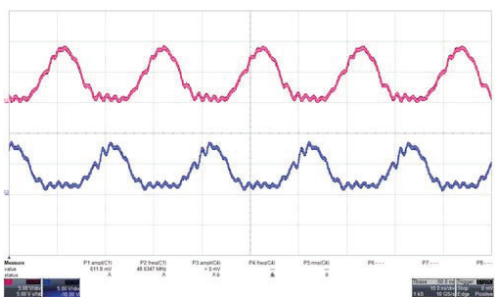
To verify the analysis presented in the paper, a 10.5 W prototype converter with regulation of the output voltage was built (see Fig. 8) and the experimental results are presented. Drain, gate, and rectifier voltages in the power stage are shown in Fig. 7. Note that the drain and rectifier voltages are measured with capacitance of 2.2 pF in series with an oscilloscope probe, in order to reduce influence of the probe to the power stage. This introduces attenuation of A = 0.19 in the measurement and removes the DC component of the measured voltages. Component values of the power stage are provided in Table I, according to a design procedure described



(a) $Av_{DS1}(t)$ and $Av_{DS2}(t)$ (scaled, no DC): 5 V/div, 10 ns/div



(b) $Av_{R1}(t)$ and $Av_{R2}(t)$ (scaled, no DC): 5 V/div, 10 ns/div



(c) $v_{GS1}(t)$ and $v_{GS2}(t)$: 5 V/div, 10 ns/div

Fig. 7: Experimental waveforms of drain, rectifier, and gate voltages in the power stage. Drain and rectifier voltages are measured with 2.2 pF capacitance in series with the oscilloscope probe (attenuated by $A = 0.19$, no DC).

TABLE I: Component list of the power stage.

Component	Value
L_{I1}, L_{I2}	Coilcraft 82 nH
L_{R1}, L_{R2}	Coilcraft 120 nH
C_{I1}, C_{I2}	80 pF (C0G)
C_{X1}, C_{X2}	18 pF (C0G)
C_{S1}, C_{S2}	–
C_{IN}	1.6 µF (X7R)
C_{OUT}	2.5 µF (X7R)
S_1, S_2	Fairchild FDC8602
D_1, D_2	NXP PMEG6010

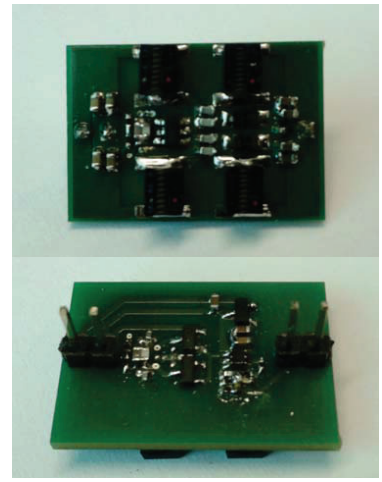


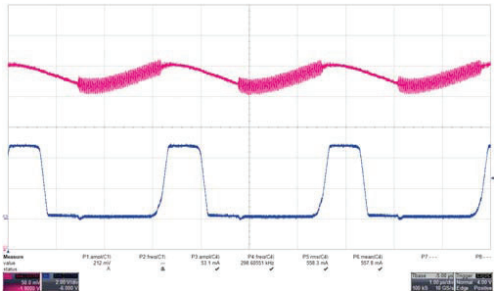
Fig. 8: Photos of the 26 mm × 18 mm 10.5 W prototype.

in [17]. Switching frequency of the power stage is $f_S = 49$ MHz. Open-loop output voltage and output voltage and current are V_{out} = 10.2 V and I_0 = 1.04 A, respectively.

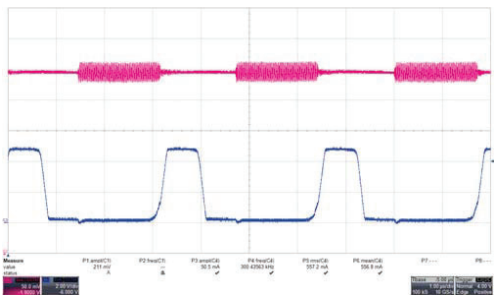
When the duty cycle of 50% is obtained, $I_{out} = 0.5\ I_0$ = 0.52 A. The waveforms of the relevant voltages in the converter for this case are shown in Fig 9. Modulation frequency f_M is at its maximum value of 300 KHz at 50% duty cycle, and drops as the duty cycle moves away from 50%. In addition, under these conditions output voltage ripple $\Delta V_{out,pp}$ is at its maximum as well.

Comparator used in the circuit is AD8468 from Analog Devices. Component datasheet specifies 40 ns propagation delay. For comparison, in [7] a high-speed TLV3501 comparator with 4.5 ns propagation delay was used, which is a reduction by a factor of 9. This is by no means a limit since there are other significant contributors as well (conditioning and power stage on-off circuit). This delay may be increased even further at a cost of a lower modulation frequency f_M and higher output voltage ripple for a given C_{out}. In addition, maximum f_M is lower in [7] compared to the one demonstrated in this work.

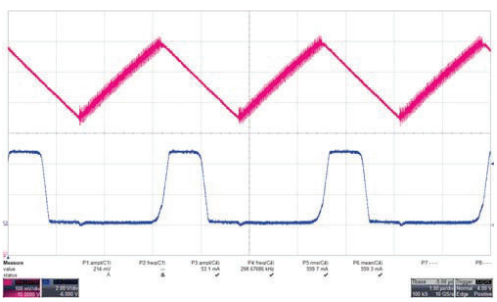
To demonstrate clearly the relationships between the signals in time domain, v_{cmp+}, v_{cmp-}, v_{GS}, v_{DS}, and v_{out} are shown in Fig. 9 and Fig. 10 (upper waveforms) with respect to the comparator output (lower waveforms). High output voltage ripple is caused by a small output filtering capacitance ($C_{out} =$ 3.3 µF). Fig. 11 shows step responses of the converter when the load is changed from 0 to 0.5 A and from 0.5 A to 0. As expected, the transient peaks in V_{out} barely exceed output voltage ripple during operation. Efficiency of the converter is shown Fig. 12 as a function of output power. Since f_M is allowed to drop significantly under light load conditions, efficiency is maintained high over wide load range ($\eta > 75\%$ above 20% load) with peak efficiency above 81%.



(a) $v_{cmp+}(t)$: 50 mV/div, 1 µs/div

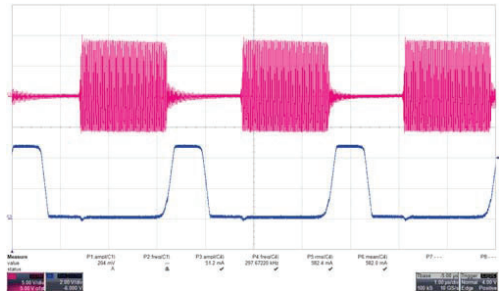


(b) $v_{cmp-}(t)$: 50 mV/div, 1 µs/div

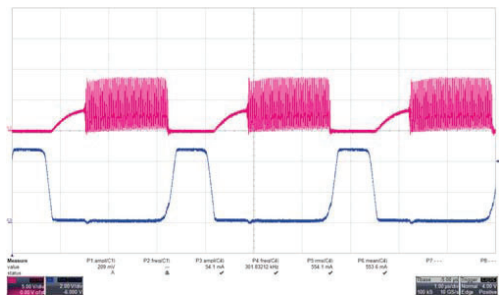


(c) $v_{out}(t)$: 100 mV/div, 1 µs/div

Fig. 9: Experimental waveforms of the control circuit with respect to $v_{cmp,out}(t)$ (2 V/div, 1 µs/div).



(a) $A\ v_{DS,AC}(t)$ (scaled, no DC): 5 V/div, 1 µs/div



(b) $v_{GS}(t)$: 5 V/div, 1 µs/div

Fig. 10: Experimental waveforms of the power stage with respect to $v_{cmp,out}(t)$ (2 V/div, 1 µs/div). $v_{DS}(t)$ is measured through a 2.2 pF capacitance.

V. Design Considerations

Since the control is based on phase shift, a small DC error is introduced in the value of V_{out}, which varies with the load. If the output voltage ripple is assumed triangular (which is justified since i_{conv} is a current square-wave), the peak values of V_{out} are determined as:

$$V_{out+} = V_{out,ref} + \frac{I_0 - I_{out}}{C_{out}}\,\Delta t_+ \tag{7}$$

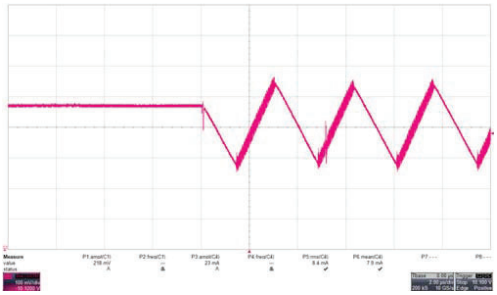
$$V_{out-} = V_{out,ref} + \frac{-I_{out}}{C_{out}}\,\Delta t_- \tag{8}$$

which gives the offset in V_{out} as

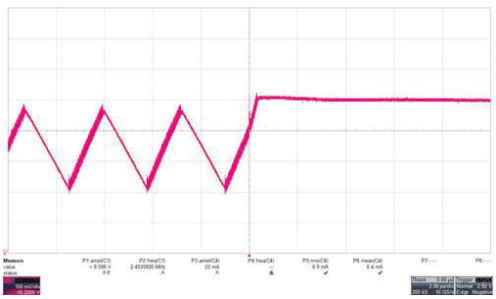
$$V_{out,offset} = V_{out,ref} - \frac{\Delta V_{out+} + \Delta V_{out-}}{2} \tag{9}$$

$V_{out,ref}$ is a target value for the output voltage set by V_{ref} and $R_{FB1} - R_{FB2}$ voltage divider. Δt_+ and Δt_- are the time delays from a point when V_{out} crosses $V_{out,ref}$ to a point where V_{out} reaches its maximum and minimum value, respectively. Depending on the variables in (7) and (8), $V_{out,offset}$ may be either positive or negative, and decreases with I_{out}. Measured dependence of ΔV_{out} is shown in Fig. 13. Both the offset and the output ripple are reduced with increase in C_{out}, while the switching frequency will be reduced.

A comparison between the model presented in section III and experimental results from section IV show close, but not perfect matching. The reasons behind this are subjects of further investigation, it is assumed that non-idealities in the active components and tolerances of the passives are the main contributors. Still, the model gives significant insight into the system operation, and can be used as a good estimate during the converter design.



(a) $v_{out}(t)$: 200 mV/div, 5 µs/div. Load step from 0 to 0.5 A.



(b) $v_{out}(t)$: 200 mV/div, 5 µs/div. Load step from 0.5 A to 0.

Fig. 11: Output voltage step response.

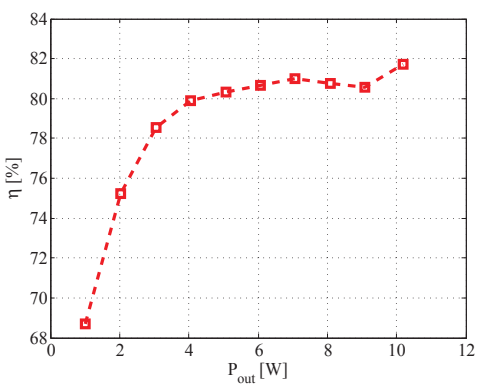


Fig. 12: Converter efficiency at $V_{in} = 24$ V.

VI. Conclusion and Future Work

In this paper, a control method for the interleaved self-oscillating resonant SEPIC converter has been analyzed and implemented. A simple model of the closed-loop system is presented along with experimental results of the implemented prototype. Burst-mode control with phase shift is chosen in order to reduce performance requirements for the comparator

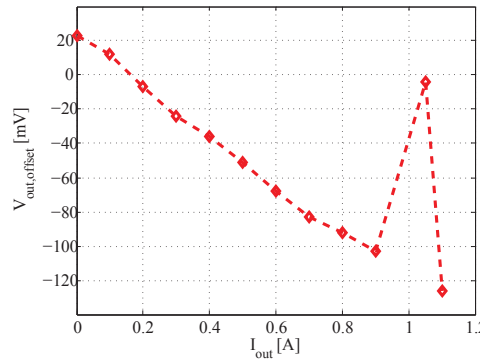


Fig. 13: Measured output voltage offset dependence on the load. At full load the modulation duty cycle is 100% and the converter runs continuously, which sets the offset back to zero. Further increase of the load causes output voltage drop.

in the control loop. Compared to hysteresis-based burst-mode control, phase shift control scheme allows use of a significantly slower and less expensive components in the control circuit, which is of importance for cost-sensitive applications such as LED lighting and PoL converters. Both the power stage and the control circuit were implemented using only low-cost commercially available components, with peak efficiency above 81% and high efficiency over wide load range.

Output voltage shows little, but observable dependence on the output load, which needs to be taken into account during converter design. This dependence may be suppressed by increasing the output capacitance, but in cost sensitive applications this may not be a desirable solution. Therefore, alternative methods of eliminating output voltage variation will be investigated.

Finally, it is of interest to look into the generated EMI of a converter using the proposed control method in order to satisfy EMC requirements.

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Appendix F

Phase-Shift Control For Very High Frequency DC-DC Converters

Submitted to IEEE Transactions on Power Electronics

Phase-Shift Control for Very High Frequency DC-DC Converters

Milovan Kovacevic, *Student Member, IEEE,* Arnold Knott, *Member, IEEE,*
and Michael A. E. Andersen, *Member, IEEE*

***Abstract*—Fast transients of very high frequency (VHF) converters allow high control bandwidths. A limitation of high bandwidth control implementations is strict requirement on delays in the feedback loop. This paper introduces a design procedure and implementation of the phase-shift burst-mode control method. The proposed control method has very high bandwidth while utilizing delays in the power stage turn-on and turn-off transitions, in order to reduce requirements for components in the control circuit. In addition, a design procedure for an interleaved self-oscillating resonant (ISOR) SEPIC converter is provided. The control method is experimentally evaluated on a 33 MHz ISOR SEPIC converter prototype. The designed converter demonstrates peak efficiency of 85%, maintains efficiency above 82% from 20% load to full load, and is implemented using low-cost power semiconductors and integrated circuits.**

***Index Terms*—on-off control, phase-shift, resonant power conversion, resonant gate drive, self-oscillating converter, very high frequency (VHF), zero voltage switching (ZVS)**

I. Introduction

CONSTANT drive for miniaturization of power converters leads inevitably to increase in converter switching frequency. As the frequency increases, passive components scale down in both physical size and value [1], [2], which permits the use of power converters in applications with severe size constraints, high performance, and fast transient response requirements. This is especially beneficial regarding magnetic components, as they are typically the biggest contributors to size and weight of power converters.

Resonant converters based on radio frequency (RF) switch-mode resonant and multi-resonant inverters and rectifiers are particularly interesting for very high frequency (VHF) dc-dc power conversion for several reasons: high efficiency and minimal switching losses, resonant operation, and low energy storage requirements. Moreover, and only a single low-side switch is required [3]–[9], with exception of class-D or LLC converter based topologies [10].

Inductance values required by these converters for operation at very high frequencies could easily be achieved with air core inductors, which offsets the size reduction, but also eliminates core loss. Lower capacitance requirements are beneficial as well, since in certain applications electrolytic capacitors limit the converter lifetime. Some of these applications are size and cost constrained (LED lights, PC power supplies,...), which potentially exposes electrolytic capacitors to operation under high ambient temperatures.

Lower energy storage values and resonant operation also lead to significantly faster transients, and therefore allow the use of on-off (or burst-mode) control techniques [5], [11]–[15]. Common control schemes for VHF power converters are pulse-width modulation (PWM) and hysteretic control method. PWM control scheme provides constant modulation frequency operation [5], but its bandwidth is considerably lower compared to hysteretic control. On the other hand, hysteretic control provides extremely high bandwidth [11], but requires short response times in all components in the feedback circuit.

This paper presents a design procedure and implementation of a burst-mode control method, which we term phase-shift control. The term is derived from phase-shift self-oscillating (SO) modulators [16], [17], used in audio applications. The method provides high control bandwidth, while absorbing and utilizing delays throughout the feedback loop. The control technique is intended for, but not limited to, output regulation of resonant [18] and quasi-resonant [19], [20] HF/VHF dc-dc converters. Properties of the control technique are evaluated on an interleaved self-oscillating resonant (ISOR) SEPIC power stage. A design procedure for the ISOR SEPIC [21] has been provided as well. The system maintains high efficiency (above 82%) from 20% load to 100% load, and 85% above 60% load. Section II describes the power stage design procedure and simulation results. Section III shows the plant and controller model and the controller design procedure. Experimental results of a 33 MHz prototype with regulated output are presented in Section IV. Finally, Section V concludes the paper.

II. Power Stage

Fig. 1 shows the proposed power stage topology, which consists of two resonant SEPIC converters [5] with capacitively cross-coupled switches S_1 and S_2 [21]–[24]. The switches are coupled in a way that the drain terminal of each switch is connected to the gate terminal of the other switch via capacitors C_{X1} and C_{X2}. These capacitors form voltage dividers with MOSFET gate to source capacitances C_{GS2} and C_{GS1}, respectively. The coupling provides oscillations in the inverter stage to start automatically when the bias voltage V_{bias} is raised above the MOSFET threshold V_{th}.

The proposed resonant gating technique is achieved with very low component count and volume (only one additional C_X and R_{bias} per converter) in the gate drive stage, and produces a half-sine voltage waveform. Other notable gating techniques with purely passive circuits are proposed in [10], [25]–[28], and produce a full-sinusoidal gate waveform.

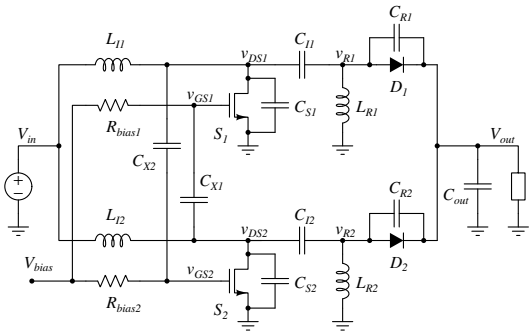

Fig. 1: Schematic of the power stage. The converter self-starts when V_{bias} rises slightly above threshold.

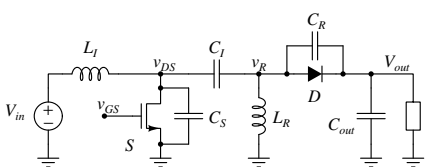

Fig. 2: Resonant SEPIC converter.

Compared to these, the proposed gate drive method generates around 50% of loss for the same peak voltage, since there is no negative half-period. In [5], [13], the resonant gate drive is half-sinusoidal function, however the implementation is more complex.

When the converter is running, drain voltage of each power stage provides the gate drive signal for the switch in the other power stage. The voltage dividers scale down the drain voltage waveform to a level appropriate for the MOSFET gates. Fig. 2 presents a single resonant SEPIC converter.

A. Design Procedure

A design procedure for a single resonant SEPIC converter has been provided in [5], which relies on a priori knowledge of the switching frequency and modulation cycle of the switch. In the proposed configuration, these values are known only approximately. Since both methods rely on approximations and require corrections to accurately match simulation, a direct synthesis method is proposed to obtain fewer number of iteration steps.

The design process begins with specifications of:

- input voltage V_{in},
- output voltage V_{out},
- output power P_{out}, and
- self-oscillating switching frequency f_S.

The first step is to select a starting value for the input inductor impedance. Self-oscillating frequency f_S is determined from the following approximate expression:

$$f_S \approx \frac{1}{2\,\pi\,\sqrt{L_I\,C_{DS,tot}}} \tag{1}$$

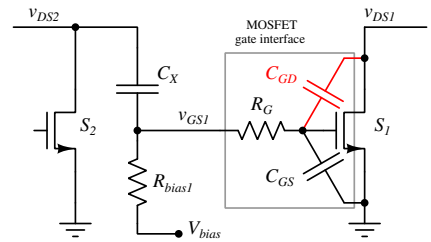

Fig. 3: Cross-coupling network: coupling from S_2 to S_1. C_{GD} is marked due to its adverse effects on operation of the gate drive scheme.

where L_I is the input inductance and $C_{DS,tot}$ is the total capacitance seen by the drain nodes when the rectifiers are shorted:

$$\begin{aligned} C_{DS,tot} &= C_I + C_{OSS} + C_S + C_X||C_{ISS} \\ C_{OSS} &= C_{DS} + C_{GD} \\ C_{ISS} &= C_{GS} + C_{GD} \end{aligned} \tag{2}$$

From (1) total drain capacitance $C_{DS,tot}$ is determined. This capacitance is split between C_{OSS}, C_I, and $C_X||C_{ISS}$. Effective drain shunt capacitance of the switching device needs to be sufficiently smaller than $C_{DS,tot}$ in order to achieve ZVS or near-ZVS. Exact value is a nonlinear function of circuit parameters, depends on nonlinearity of switching devices' junction capacitances, and therefore difficult to obtain analytically. However, a good starting point is if drain to source shunt capacitance, $C_{DS,tot} - C_I$, is smaller than $C_{DS,tot}/2$.

Once the switching device is selected, the next step is to determine coupling capacitance C_X. Assuming perfect symmetry between the converters, and small gate resistance impedance is small, $v_{GS1}(t)$ and $v_{GS2}(t)$ are given as:

$$\begin{aligned} v_{GS1,2}(t) = v_{DS2,1}(t)\,&\frac{C_X}{C_{GS}+C_{GD}+C_X} + \\ + v_{DS1,2}(t)\,&\frac{C_{GD}}{C_{GS}+C_{GD}+C_X} + \\ + V_{bias} \end{aligned} \tag{3}$$

Fig. 3 shows the cross-coupling network. The first term in (3) is the targeted capacitive cross-coupling from one converter's switch to the other. C_X needs to be selected such that the desired gate voltage amplitude V_{GS} is achieved. The second term is the voltage reflection from drain to gate of the same switch through C_{GD}. This term is undesirable, as it may cause accidental partial or full turn-on of the MOSFET, which may cause high loss, significant lifetime reduction, or destruction of the switch if C_{GD} is nontrivial compared to C_{ISS}. In ISOR SEPIC, $V_{DS,p-p}$ is typically close to 3 V_{in}. If $C_X \gg C_{GD}$ at higher voltages, for a given peak gate voltage $V_{GS,p-p}$ is obtained from (3) as:

$$C_X = \frac{C_{GS}+C_{GD}}{\frac{V_{DS,p-p}}{V_{GS,p-p}} - 1} \tag{4}$$

It is important to note that C_{GD} in (4) is at $v_{DS} = 0$. C_I

is determined from (2) once all the other drain capacitances are known. Normally, no additional shunt capacitance C_S is required. However, it will undoubtedly appear in practical implementation, which may cause disagreement between designed converter and experiment. Since the converter switching frequency is primarily determined by L_I and $C_{DS,tot}$, the converter actual performance is very sensitive to their variations.

The diode is chosen such that it meets voltage blocking and current handling requirements, while keeping the capacitance and reverse recovery time to a minimum. Typically, Schottky diodes are used at very high frequencies since they ideally do not exhibit reverse recovery effects.

The rectifier inductance L_R is iteratively adjusted via simulation until the converter is at a boundary between ZVS and non-ZVS operation. A good starting value for iterations is in range 1-2 $\cdot L_I$. It should be noted that very low L_R/L_I ratio may lead to different modes of oscillation, which are suboptimal compared to the conventional resonant SEPIC mode.

Finally, the converter impedances need to be scaled to meet the specified P_{out}, and fine-tune f_S if necessary. If all waveform shapes need to be maintained exactly, proper scaling of all reactive elements and semiconductors is required. The minimum set of impedances is Z_{L_I}, Z_{L_R}, and Z_{C_I}.

B. Design Considerations

There are several important points for the design process:

1) In all power MOSFETs, $C_{GD}(v_{DS})$ curve decreases rapidly with v_{DS}, therefore the parasitic voltage reflection from drain to gate terminal of the same device is reduced. The property reduces the danger of accidental device turn-on at high v_{DS}. Still, high capacitance value at low v_{DS} may affect the gate peak to peak value.
2) MOSFET threshold decreases with junction temperature, which may start causing high loss or destruction of the device if the turn-off gate voltage level is close to V_{th}. If the voltage reflection through C_{GD} is nontrivial (v_{GS} in the MOSFET off state changes by several volts), C_X needs to be increased accordingly, and adding extra capacitance in parallel to C_{GS} should be considered.
3) Even though no additional C_S or C_R capacitances are required, they will certainly appear in implementations as parasitics and cause disagreement between designed converter and experiment. The same applies to parasitic inductances introduced by PCB traces. In general, as the switching frequency go up and parasitics become comparable in size with the circuit elements, it becomes increasingly difficult to match simulations and experiment without rigorous modeling of all circuit components. Since the converter switching frequency is primarily determined by L_I and $C_{DS,tot}$, the converter actual performance is the most sensitive to their variations.
4) In certain Schottky diodes, p-type guard ring that prevents breakdown around edges of Schottky metal to n-type semiconductor contact may start conducting current. Since the guard ring forms a p-n junction with substrate and therefore suffers from reverse recovery effects, the diode and the converter performance is adversely affected. Commercial power Schottky diodes are not tested for operation at VHF, making the proper device choice tedious.

C. Numerical Example

To demonstrate the power stage design procedure, a power stage is designed with the following specifications:

- input voltage: $V_{in} = 24$ V
- output voltage: $V_{out} = 10.5$ V
- output power: $P_{out} = 11$ W
- switching frequency: $f_S = 33$ MHz

Starting impedance of L_I of 25 Ω is chosen, which yields $L_I = 120$ nH and $C_{DS,tot} = 193$ pF.

Peak MOSFET drain voltage is expected to reach $3 \cdot V_{in} =$ 72 V. Therefore, a 80-100 V rated switching device is required. FDC8602 from Fairchild Semiconductor was selected as the main switch since it meets voltage requirements, has low C_{OSS} and C_{ISS} (around 45 pF and 70 pF, respectively), and low $R_{DS,on}$ (350 mΩ at 10 V) compared to switching devices of similar size. Moreover, C_{GD} at high voltage is below 1 pF, which essentially guarantees very small voltage reflection onto the device gate from its drain node. In addition, R_G is only 1.6 Ω (typical values range from 0.5 Ω to 7 Ω), which is important from the gate loss standpoint.

With $C_{ISS} = 70$ pF, for $V_{GS,pp} = 12$ V, C_X needs to be at least 15 pF. This leaves approximately 135 pF for C_I. In practice, small parasitic $C_{GS,pcb}$ and $C_{DS,pcb}$ will affect the calculated values. For example, if there was 5 pF for both of these values, C_X should be increased by 1 pF and C_I reduced by 6 pF.

PMEG Schottky diode family is chosen due to its low parasitic capacitance and excellent performance in recent VHF designs. In particular, PMEG6010 meets expected voltage blocking requirement of 3.5-4 V_{out} and average current rating. Starting value for the rectifier inductor L_R of 190 nH is chosen.

The designed power stage is simulated in SPICE and characteristic waveforms are shown in Fig. 4. For the specified V_{in} and V_{out}, the resulting P_{out} and f_S are 12.4 W and 33.2 MHz, respectively. To compensate for the difference, C_I is reduced to 117 pF, and new simulation reported 10.97 W and 34.5 MHz. We proceed with the new value since we decided to err on the side of frequency rather than output power, because parasitics in the experimental setup are expected to slightly reduce the switching frequency. Efficiency of the simulated converter is 85.3%. All inductors are simulated with Q factors of 130, which is common for air-core inductors of similar size from Coilcraft 2222SQ series at the frequency of interest. Compared to the specifications, switching frequency is higher by less than 4.6% and output power is within 0.3%, therefore no additional modifications are deemed necessary. It is however possible to improve the design further by using an optimization tool and more precise models of the semiconductor devices.

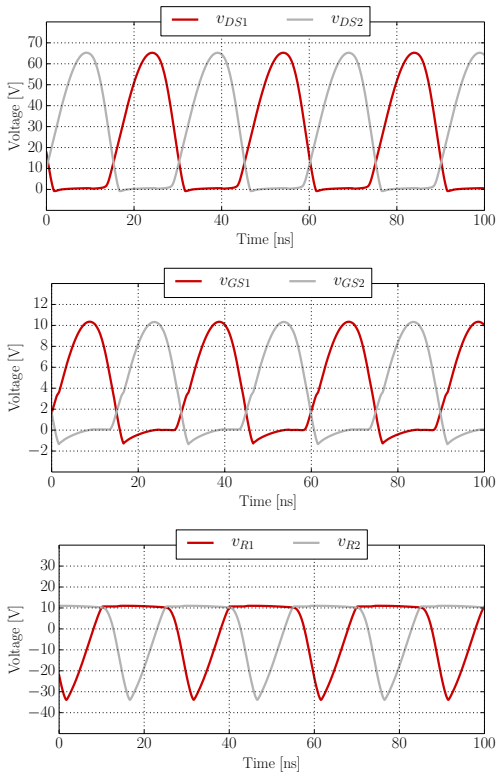

Fig. 4: Simulated waveforms of the designed power stage. From top to bottom: drain, gate, and rectifier voltages.

III. Control Scheme

The phase-shift control is a burst-mode control method based on utilizing delays in the feedback circuit to generate turn-on and turn-off pulses for the power stage. It is similar to hysteretic control method, with the hysteresis being in time domain instead of voltage domain. This allows the use of components which have significantly higher propagation delays compared to hysteretic control in the feedback loop.

A. Method Overview and Implementation

On-off or burst-mode control methods for dc-dc converters rely on two main assumptions: the converter dynamics are significantly faster compared to the modulation frequency, and the energy stored in the magnetics is much smaller compared to the energy stored in the output capacitor. This is true for both conventional dc-dc converters that operate in discontinuous conduction mode (DCM), resonant converters in general, and VHF converters in particular. Since the output voltage is tightly regulated, and if switching frequency ripple is neglected, the converter output can be modeled as a constant current source with the current I_0. When an on/off modulation

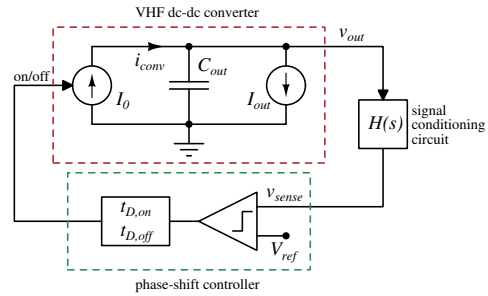

Fig. 5: Low frequency system model of a VHF converter with a phase-shift controller.

is applied, the current delivered by the converter i_{conv} to C_{out} and the load is approximately modeled as a current square-wave:

$$i_{conv} = \begin{cases} I_0, & \text{when the converter is ON} \\ 0, & \text{when the converter is OFF} \end{cases} \tag{5}$$

Output current I_{out} is equal to an average value of i_{conv} over one modulation cycle. The resulting current going into C_{out} is $i_{conv} - I_{out}$, which has no DC component in steady state. If parasitics of C_{out} are negligible, the resulting v_{out} voltage waveform is a triangular wave. Assuming that turn-on and turn-off delays are independent of the output voltage rate of change, The output voltage ripple is

$$\Delta V_{out} = \frac{I_{out}}{C_{out}}\, t_{D,on} + \frac{I_0 - I_{out}}{C_{out}}\, t_{D,off} \tag{6}$$

where $t_{D,on}$ and $t_{D,off}$ are the converter turn-on and turn-off delays, respectively. If the controller's delays are constant, (6) shows that ΔV_{out} is a linear function of I_{out}, and the longer delay defines $\Delta V_{out,max}$. In the special case when $t_{D,on}$ and $t_{D,off}$ are equal, ΔV_{out} is independent of I_{out}. At any given load, by knowing C_{out} and propagation delays, v_{out} and f_M are determined:

$$\Delta V_{out,off} = \frac{\Delta V_{out}}{2}\, \frac{t_{D,on} - t_{D,off}}{t_{D,off} + t_{D,on}} \tag{7}$$

and

$$f_M = \frac{I_0}{C_{out}\, \Delta V_{out}}\, \frac{I_{out}}{I_0} \left(1 - \frac{I_{out}}{I_0}\right) \tag{8}$$

Modulation frequency is highest at 50% load:

$$f_{M,max} = \frac{1}{2\,(t_{D,on} + t_{D,off})} \tag{9}$$

Fig. 5 presents a low frequency model of the complete system. The signal conditioning circuit scales V_{out} to a level suitable for the comparator, and possibly provide noise filtering. Depending on the implementation, it may or may not introduce delay in the feedback loop. The control circuit is composed of a comparator with converter driver circuitry, which allows turn-on and turn-off of the converter. $t_{D,on}$ and $t_{D,off}$ are the turn-on and turn-off delays are contributions

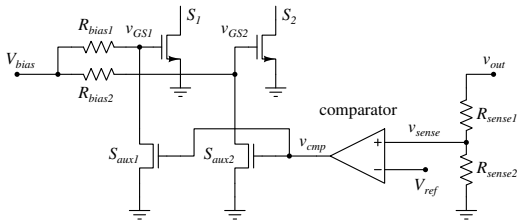

Fig. 6: Phase-shift burst-mode controller implementation for interleaved self-oscillating resonant SEPIC converter.

from both the comparator and the converter driver.

Fig. 6 shows the proposed control circuit for the interleaved self-oscillating resonant SEPIC converter. Feedback is taken to the comparator from the output voltage through a voltage divider $H(s)$, formed by R_{sense1} and R_{sense2}

$$H(s) = \frac{R_{sense2}}{R_{sense1} + R_{sense2}} \tag{10}$$

The comparator turns the switches S_{aux1} and S_{aux2} on and off, according to the voltage difference at its input. When S_{aux1} and S_{aux2} are on, v_{GS1} and v_{GS2} are zero and the oscillations are inhibited. Once S_{aux1} and S_{aux2} are off, v_{GS1} and v_{GS2} start to increase from 0 to V_B as device gate capacitances are charged through R_{bias1} and R_{bias2}. When v_{GS1} and v_{GS2} exceed the power MOSFET threshold voltage V_{th}, switches S_1 and S_2 enter saturation and initiate oscillations in the power stage.

Note that $C_{OSS,aux}$ (3 pF) is in parallel to C_{ISS} (70 pF) of the corresponding power device. In this work $C_{ISS} \gg C_{OSS,aux}$, but when that is not the case relation (2) needs to include this term as well.

B. Design Considerations

The signal conditioning circuit in Fig. 6 provides voltage scaling only. Depending on the particular implementation of the power stage and the controller, a more elaborate network may be implemented. Shunt capacitance in parallel to R_{sense2} may be added to provide additional noise filtering and phase shift. However, adding significant phase shift in this way should be avoided, as it tends to decrease the signal level at the sense node. It is therefore more appropriate to provide additional phase shift after the comparator. Capacitance in parallel to R_{sense1} may be added to provide more AC signal coupling into the feedback node. In this work, no additional signal conditioning was required.

The analysis above assumes a comparator-based controller with no voltage hysteresis. Typically, comparators are made with a built-in hysteresis of few mV, which serves to reduce "chattering" of the comparator's output in noisy environments, in particular when the slopes are very slow. In addition, delays are functions of overdrive voltage, and therefore of the rate of change of the input signal. Both of these effects extend the delay on during slow input voltage change, while not affecting faster changes significantly - thus reducing V_{out} variation at the extremes of load range.

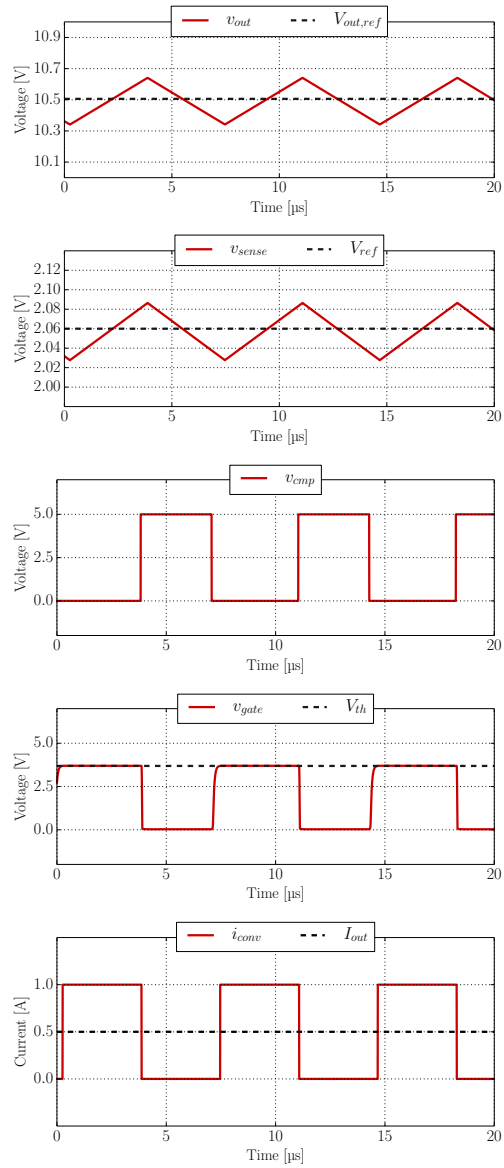

Fig. 7: Simulated characteristic voltage and current waveforms of the model from Fig. 5.

C. Numerical Example

Design of a phase-shift burst mode controller begins with specifications for:

- output voltage $V_{out} = 10.5$ V
- allowed output voltage ripple: $\Delta V_{out} = 300$ mV
- maximum modulation frequency: $f_{M,max} = 140$ kHz

- maximum output load current: $I_{out,max} = 1$ A

Converter output current I_0 is also set to 1 A, which implies that $f_{M,min} = 0$. To obtain $f_M > 0$, the $I_0 > I_{out,max}$ condition needs to be satisfied. In addition, a minimum load needs to be always present as well. Assuming that $t_{D,on} - t_{D,off} = 400$ ns, $t_{D,on}$ and $t_{D,off}$ are obtained from (6):

C_{out} is solved from (8) for $f_M = f_{M,max}$, $I_{out} = I_0/2$, and equals 6.0 µF. Expression (9) determines the average delay in the circuit $(t_{D,on} + t_{D,off})/2$ = 1.79 µs. Assuming that $t_{D,on} - t_{D,off}$ is around 400 ns and substituting in (6), we can verify if ΔV_{out} specification is satisfied. Since the turn-on delay is longer, ΔV_{out} is higher at high modulation cycles. To compensate, C_{out} needs to be increased to 6.35 µF, assuming no change in time delays and modulation frequency.

This is because shutdown is performed by the auxiliary switches S_{aux1} and S_{aux2}, while during startup C_{ISS1} and C_{ISS2} are passively charged from the bias voltage source V_{bias} through the biasing resistors.

In Fig. 7, characteristic voltage and current levels from a numerical example of the model are shown, where:

- C_{out} = 6.0 µF
- I_0 = 1.0 A, I_{out} = 0.5 A
- $V_{ref} = 2.06$ V
- R_{sense2} = 2 kΩ, R_{sense1} = 8.2 kΩ
- $t_{D,on}$ = 1.59 µs + 0.4 µs = 1.99 µs
- $t_{D,off}$ = 1.59 µs

$v_{gate}(t)$ represents the gate voltages of S_1 and S_2 with removed VHF component. $V_{out}(t)$ passes through the voltage divider $H(s)$, resulting in a triangular waveform $v_{sense}(t)$. Average value of $v_{sense}(t)$ is slightly lower than the referent V_{ref} voltage, which is due to $t_{D,on} > t_{D,off}$. This is also the cause of the duty cycle of the comparator output $v_{cmp}(t)$ to be lower than 50%. Since the referent output voltage $V_{out,ref}$ is 10.5 V, a small offset can be observed in $v_{out}(t)$.

IV. Experimental Results

To demonstrate effectiveness of the proposed approach, an experimental setup was built and the results are presented. The setup consists of an interleaved self-oscillating resonant SEPIC converter, operating at 33 MHz, and the phase-shift controller. The controller regulates the output voltage to 10.5 V. The prototype is shown in Fig. 8.

A. Power Stage

Fig. 9 shows important voltage waveforms of the free-running power stage. The respective waveforms in the two resonant SEPIC converters are very well balanced and 180° out of phase. While free-running, the converter operates at 85.2% efficiency and delivers 10.82 W. Components used in the power stage are listed in Table I.

Performance of the experimental converter is very similar to the design example in Subsection II-C, with few notable differences. Inductances L_I and L_R are 110 nH and 180 nH instead of 120 nH and 190 nH, as 5-10 nH of parasitic inductance were expected from the PCB traces. Parasitic $C_{S,pcb}$, $C_{GS,pcb}$, and $C_{R,pcb}$ are measured on an unpopulated board and are 5.0 pF, 3.5 pF, and 4.5 pF, respectively. C_X is also made larger - 18 pF instead of 15 pF, which is 17% higher compared to the value in the design. Since C_X is composed of NP0 capacitors, this suggests that the effective C_{ISS} is larger than predicted. Note that the oscilloscope probe adds 8.0 pF of capacitance during measurement, which reduces the observed gate voltage amplitude as well.

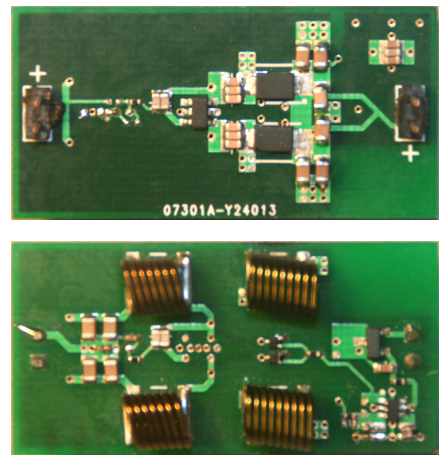

Fig. 8: 33 MHz, 10.87 W experimental prototype with phase-shift controller. Dimensions: 20.2 mm × 40.6 mm.

TABLE I: Power stage component list.

Component	Value
L_{I1}, L_{I2}	Coilcraft 110 nH
L_{R1}, L_{R2}	Coilcraft 180 nH
C_{I1}, C_{I2}	117 pF (C0G)
C_{X1}, C_{X2}	18 pF (C0G)
C_{S1}, C_{S2}	–
C_{in}	4 × 680 nF (X7R)
C_{out}	12 × 680 nF (X7R)
S_1, S_2	Fairchild FDC8602
D_1, D_2	NXP PMEG6010

The simulation from Section II-C is updated with the observed differences, and yields $P_{out} = 10.9$ W and $f_S = 33.5$ MHz. Table II shows loss distribution in the simulation and compares to the total loss measured in the experimental converter. The loss contributed by circulating currents in C_{OSS} and C_D we term "displacement" loss. Calculated and measured loss and efficiency match to 4.5%, even though simple models are used. Rigorous thermal and electrical analysis is required to confirm the loss distribution from Table II. Due to complexity of the problem, such modeling falls outside of scope of this publication.

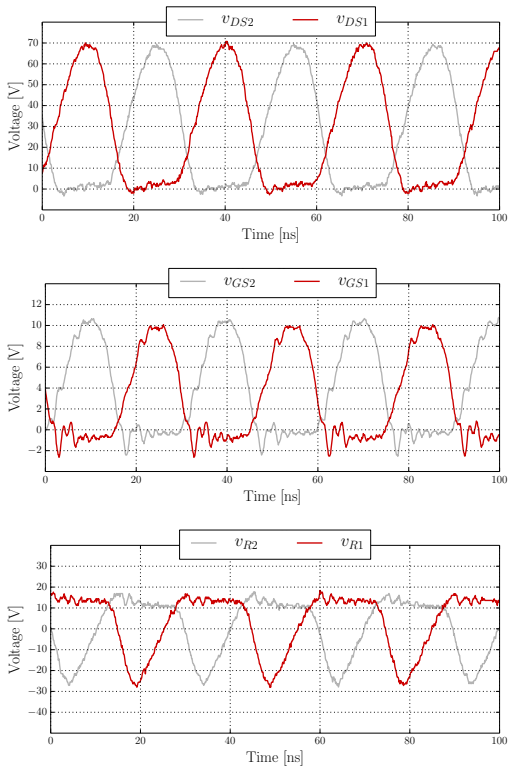

Fig. 9: Measured power stage drain (top), gate, and rectifier (bottom) waveforms with $V_{in} = 24$ V and $V_{out} = 10.5$ V. All waveforms are captured with the same time reference.

In general, to have a near-perfect match between simulation and experiment, a very careful impedance profiling and device modeling needs to be performed. Still, the simple model and the proposed approach are in good agreement in all performance parameters.

B. Phase-Shift Controller

Voltage waveforms shown in Fig. 10 present the converter operation at 50% load. f_M is at its maximum of 142 kHz, while ΔV_{out} is very close to 300 mV, thus matching the design example from Section III-C. However, C_{out} is 26% smaller in the design, and the combination of ΔV_{out}, f_M, and I_0 suggests that the effective C_{out} in the experimental setup is actually around 6.0 µF. This can be partially explained by the fact that capacitance of X7R capacitors decreases with voltage and aging, although a smaller difference (around 10-15%) for 50 V rated capacitors was expected.

The comparator used in the phase-shift controller is NCX2200, with typical propagation delay of 800 ns and typical hysteresis voltage of 9 mV. Due to low signal levels, low slope of v_{sense}, and presence of hysteresis, effective delay

TABLE II: Power loss breakdown.

Component	Calculated	Measured
L_{I1}, L_{I2}	2 × 248 mW	–
L_{R1}, L_{R2}	2 × 114 mW	–
C_{I1}, C_{I2}	≈ 0	–
C_{X1}, C_{X1}	≈ 0	–
$R_{bias}1$, $R_{bias}2$	2 × 24 mW	–
S_1, S_2: conduction	2 × 140 mW	–
S_1, S_2: gating	2 × 16 mW	–
S_1, S_2: displacement	2 × 31 mW	–
C_{in}	≈ 0	–
C_{out}	≈ 0	–
D_1, D_2: conduction	2 × 365 mW	–
D_1, D_2: displacement	2 × 45 mW	–
control circuit (idle)	11 mW	–
Total	1.98 W	1.89 W
Relative to P_{out}	15.3%	14.8%

at 50% modulation cycle is close to 1550 ns, which is an increase of 94%. Datasheet [29] provides insight into this issue: propagation delays t_{PHL} and t_{PLH} are measured with a square wave 50 mV and 100 mV overdrive. For the same temperature and supply voltage, the delays are 50% larger for 50 mV overdrive. It is therefore reasonable to assume that the delays are even longer for a triangle wave. However, order of magnitude is important to capture, as it is the basis for comparison.

Start-up and shut down transitions are shown in Fig. 11 and Fig. 12. It is apparent that a delay exists between the comparator falling edge (enable) and the actual start of the converter. The delay is due to passive nature of the start-up, as explained in Section III. The converter enters steady state within 6-7 switching cycles, and experiences non-ZVS for maximum 2-3 cycles. Shut-down of the converter is almost instant with respect to the rising edge of v_{cmp}, and happens within one switching cycle. An unusual artifact appears at the falling edge of the comparator's output. Since the output is loaded with high impedance (≈ 2 kΩ) at all times, the most likely cause for such artifact is partial cross-conduction in its output stage due to delayed turn-off of the upper MOSFET. Regardless of the actual cause, the artifact did not cause any significant penalty on the converter operation.

Load step transitions from 0% to 50% load and from 50% to 0% load are shown in Fig. 13. As expected, the controller quickly adapts and maintains control of the output voltage within one turn-on or turn-off delay period.

Converter efficiency over the load range is shown in Fig. 14. The converter is more than 80% efficient above 10% load, and maintains 85% efficiency above 60% load. Fig. 15 presents the output voltage variation with load. As expected, average value

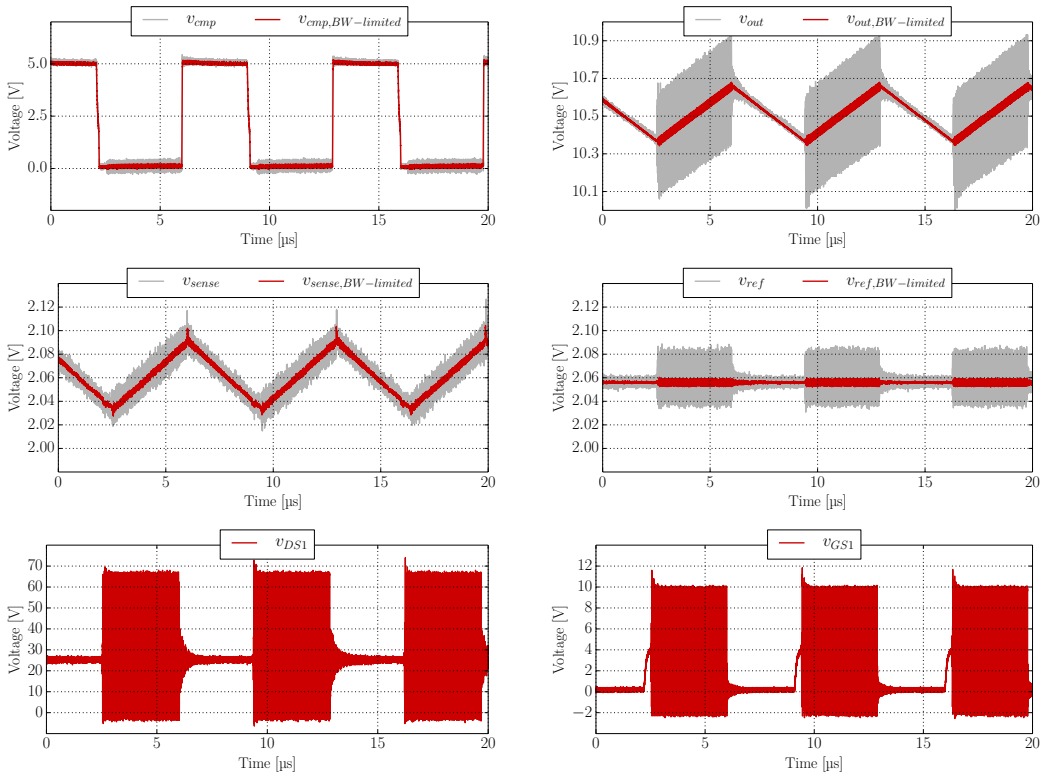

Fig. 10: Experimental waveforms in steady state with 50% load. v_{cmp}, v_{out}, v_{sense}, and v_{ref} are shown with (red) and without (gray) 20 MHz bandwidth limit on the oscilloscope. v_{DS} and v_{GS} are measured with full bandwidth (500 MHz, limited by oscilloscope probes). In the following figures v_{out} and v_{cmp} are shown with 20 MHz bandwidth limit only.

of V_{out} decreases as the load increases. However, the variation is within 100 mV, which is tolerable in many applications. From Fig. 15 we determine the output impedance of the converter:

$$Z_{out} = \frac{\Delta V_{out}}{\Delta I_{out}} = \frac{0.1\ \text{V}}{0.8\ \text{A}} = 0.13\ \Omega \tag{11}$$

Above $I_{out} = 1.03$ A the modulation cycle reaches 100% and the converter moves towards operating points with less optimal performance. This is due the fact that the switching frequency stays roughly the same, causing the same circulating currents in the inverter side, while the power delivery is reduced. Therefore, both the converter efficiency and output voltage start to drop.

In Fig. 16, the converter and comparator outputs are shown at 50% load when extra 150 µF is added to the output capacitance. Output voltage ripple is reduced to 70 mV peak to peak, however the modulation frequency dropped to 41 kHz, which suggests that there is a voltage dependence on propagation delays in the comparator. This effect is explained by the presence of a small built-in hysteresis at the comparator input. In fact, the in-built hysteresis turns the pure phase-shift control method into a hysteresis/phase-shift hybrid control law, in which the hysteresis part gains on importance as $\mathrm{d}v_{sense}/\mathrm{d}t$ is reduced due to output voltage drop. Nevertheless, Fig. 16 demonstrates that the control method is robust and is capable of performing even with very low $\mathrm{d}v_{sense}/\mathrm{d}t$. The ripple observed at the power stage start-up and shut-down is due to resonance between parasitic inductance of the electrolytic capacitor and ceramic capacitance.

C. Comparison with State-of-The-Art

It is of interest to compare the controller performance from this work against recent achievements, while taking into account different power levels and operating frequencies. Table III shows the controller performance comparison.

In [11] and [13] hysteretic controllers are used with 30 MHz and 110 MHz power stage, respectively. In [11], calculation reveals that impedance of C_{out} at 150 kHz is much larger than $(2\pi f_M C_{out})^{-1}$, meaning that the parasitics dominate the electrolytic capacitor impedance, and that an equivalent 16.5 µF capacitance with low parasitics yields the same

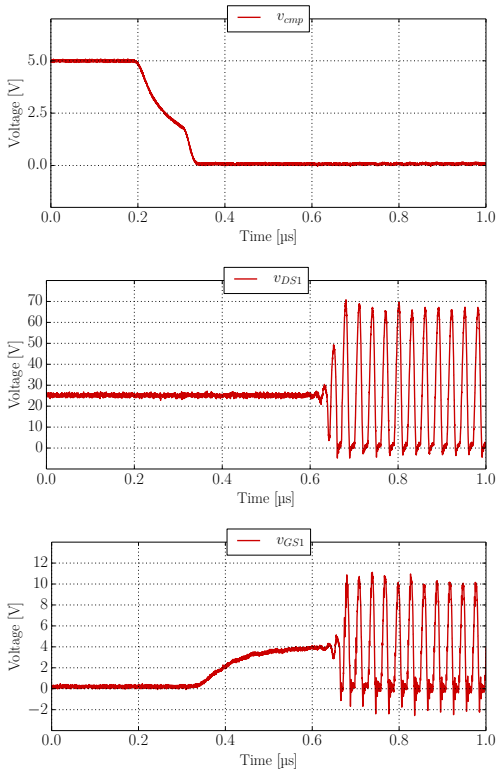

Fig. 11: Start-up transition of the experimental converter. From top to bottom: comparator output, drain voltage, gate voltage waveforms. The comparator falling edge is unusual and seems to be a property of its output stage, most likely the top-side MOSFET didn't turn off immediately. Apart from adding extra delay during the converter start-up, it causes no adverse effects.

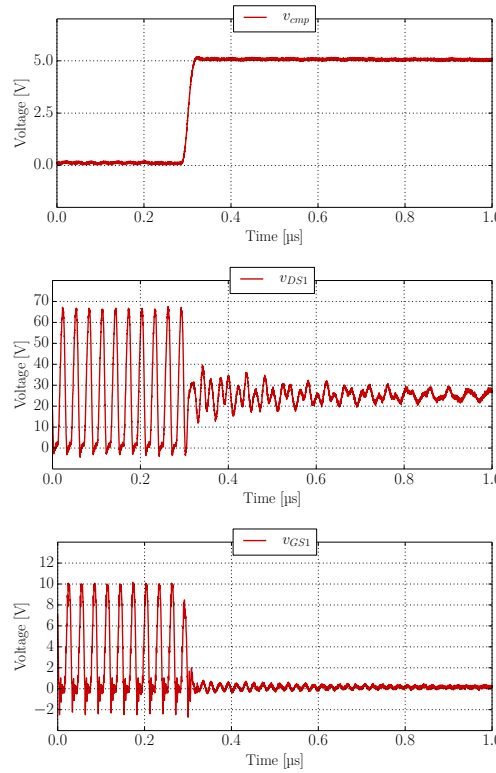

Fig. 12: Shut-down transitions of the experimental converter. From top to bottom: comparator output, drain voltage, gate voltage waveforms.

performance. The same reasoning applies for [13], where equivalent capacitance is 17.5 µF.

In order to provide a fair comparison, we use the following parameters: $\Delta V_{out}/V_{out}$, $\Delta V_{out,p-p}/I_{out}$, and $t_{D,nom}/T_S$. $t_{D,nom}/T_{M,max}$ represents nominal delay in the comparator relative to minimum modulation period. From Table III we conclude that controller #2 provides superior $\Delta V_{out}/V_{out}$ (4.6 times smaller), but has nearly the same $\Delta V_{out,p-p}/I_{out}$ as shown in this work. This implies high sensitivity of the used comparator. On the other hand, $\Delta V_{out,p-p}/I_{out}$ is nearly 3 times smaller in controller #1, with 36% better $\Delta V_{out}/V_{out}$ relative to the phase-shift controller. Note, however, that $\Delta V_{out}/V_{out}$ and $\Delta V_{out}/I_{out}$ parameters are well within one order or magnitude of difference. The main comparator in both [11] and [13] is TLV3501 from Texas Instruments with typical propagation delay of 4.5 ns, which is 178 times (more than two orders of magnitude) faster compared to NCX2200. In addition, theoretical $t_{D,nom}/T_{M,max}$ ratio for the phase-shift controller at 50% load is 25%, clarifying that NCX2200 propagation delay is longer than 800 ns due to slow rise/fall times of v_{sense} voltage.

Therefore, we conclude that hysteretic and phase-shift controller with a comparator of equal sensitivity are matched in performance even with two orders of magnitude of difference in propagation delay.

V. Conclusion

Higher switching frequencies offer numerous advantages over the conventional power converter designs: smaller size and weight, higher power density, easier output control due to simple low frequency behavior, and high control bandwidth and fast transient response. To achieve these goals, high-end components and high cost are required.

This document presents an on-off control method, which we term phase-shift control method, that achieves these high performance goals. The method utilizes delays in the feedback loop in order to reduce fast response requirements on the controller components and the power stage. The method is implemented alongside a power stage which uses low-cost,

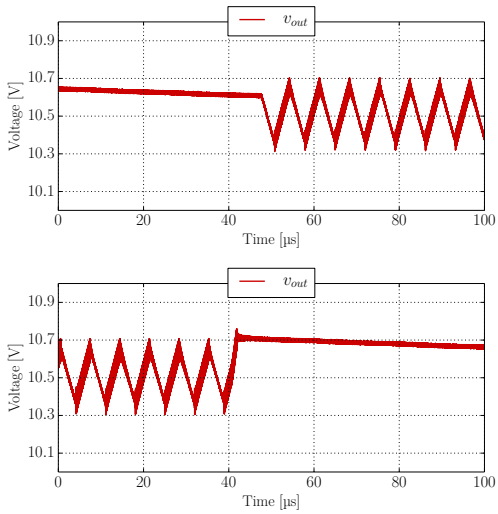

Fig. 13: Converter transient response for load change from 0 to 50% (top) and from 50% to 0 (bottom). Slow voltage decay at 0% load is due to current in the sense resistors and the control circuit.

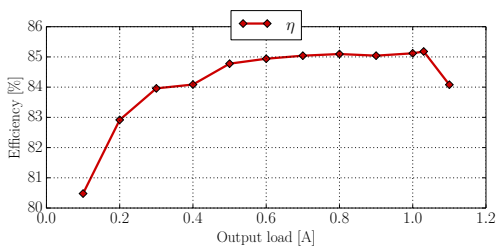

Fig. 14: Converter efficiency versus I_{out}.

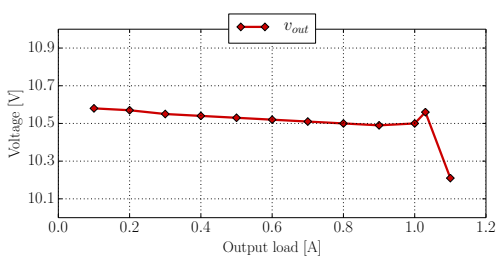

Fig. 15: Output voltage dependence on I_{out}.

commercially available components and switches, and minimum gate driver circuitry. Experimental results demonstrating the control method and power stage implementation are presented. The results are comparable to hysteretic control implementations with two orders of magnitude faster reaction times.

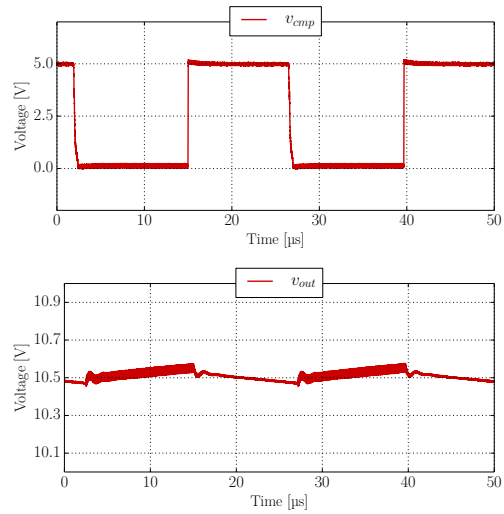

Fig. 16: The comparator and converter outputs when C_{out} is increased by 150 µF (electrolytic) capacitance. Voltage ringing in v_{out} is caused by resonance between series inductance of the electrolytic capacitor and the ceramic capacitor.

TABLE III: Controller performance comparison at 50% load.

Parameter	Hyst. #1	Hyst. #2	Phase-shift
$f_{M,max}$	150 kHz	50 kHz	142 kHz
V_{out}	33.0 V	32.5 V	10.5 V
I_{out}	3.0 A	0.36 A	0.52 A
$\Delta V_{out,p-p}$	0.6 V	0.2 V	0.3 V
C_{out}	2200 µF	40 µF	8.16 µF
$C_{out,eff}$	16.5 µF	17.5 µF	6.0 µF
$t_{D,nom}$	4.5 ns	4.5 ns	800 ns
$\frac{\Delta V_{out,p-p}}{V_{out}}$	1.82%	0.62%	2.86%
$\frac{\Delta V_{out,p-p}}{I_{out}}$	0.20 V/A	0.57 V/A	0.59 V/A
$t_{D,nom}/T_{M,max}$	0.067%	0.023%	11.36%

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Milovan Kovacevic (S'13-M'15) received the B.Sc.E.E. and M.Sc.E.E. degrees from the University of Belgrade, Serbia, in 2008 and 2010, respectively. He is currently pursuing his Ph.D. degree at the Technical University of Denmark, Kgs. Lyngby, Denmark, in collaboration with FINsix Corporation, Menlo Park, California.

He is engaged in research in the area of high frequency power electronics. His research interests are in power electronics, resonant converters, soft-switching topologies, analog and mixed-signal electronics, and control techniques of power converters.

Arnold Knott (M'10) received the Diplom-Ingenieur (FH) degree from the University of Applied Sciences in Deggendorf, Germany, in 2004. From 2004 until 2009 he has been working with Harman/Becker Automotive Systems GmbH in Germany and USA, designing switch-mode audio power amplifiers and power supplies for automotive applications. In 2010 he earned the Ph.D. degree from the Technical University of Denmark, Kongens Lyngby, Denmark working on a research project under the title "'Improvement of out-of-band Behaviour in Switch-Mode Amplifiers and Power Supplies by their Modulation Topology"'. From 2010 to 2013 he was Assistant Professor and since 2013 Associate Professor at the Technical University of Denmark. His interests include switch-mode audio power amplifiers, power supplies, active and passive components, integrated circuit design, acoustics, radio frequency electronics, electromagnetic compatibility and communication systems.

Michael A. E. Andersen (M'88) received the M.Sc.E.E. and Ph.D. degrees in power electronics from the Technical University of Denmark, Kongens Lyngby, Denmark, in 1987 and 1990, respectively. He is currently a Professor of power electronics at the Technical University of Denmark. Since 2009, he has been Deputy Head of Department at the Department of Electrical Engineering. He is the author or coauthor of more than 200 publications. His research interests include switch-mode power supplies, piezoelectric transformers, power factor correction, and switch-mode audio power amplifiers.

Appendix G

VHF Series-Input Parallel-Output Interleaved Self-Oscillating Resonant SEPIC Converter

IEEE Energy Conversion Congress and Exposition (ECCE 2013, CO, USA)

VHF Series-Input Parallel-Output Interleaved Self-Oscillating Resonant SEPIC Converter

Milovan Kovacevic, Arnold Knott, Michael A. E. Andersen
Department of Electrical Engineering
Technical University of Denmark
Kgs. Lyngby, Denmark
Email: {mikov, akn, ma}@elektro.dtu.dk

***Abstract*—If the switches of two resonant SEPIC converters are capacitively coupled, it is possible to obtain a self-oscillating converter in which the two power stages operate in interleaved mode. This paper describes a topology where the inputs of two SEPIC converters are connected in series, thereby sharing the input voltage. For the same output power and switching frequency, the voltage stress of the switches is reduced by a factor of two while the voltage transformation ratio is doubled. This modification is possible with addition of only two capacitors in the power stage and a biasing circuit. Design considerations and challenges are investigated. To verify the proposed design, a 70 V input, 37 MHz prototype was built using low-cost switching and passive components, and experimental results are presented. Peak observed efficiency was 82%.**

I. Introduction

Reducing the physical size of electronic equipment in power applications is desired in order to add more features into existing products, integrate power converters in places normally unfit for such equipment, and reduce system cost. Increasing the operating frequency of the converter is a direct way of reducing the size of energy storage elements such as bulky capacitors and inductors, which usually dominate the overall converter volume.

However, the challenges that arise when the converter operating frequency is increased into the Very High Frequency (VHF) band ranging from 30 MHz to 300 MHz are numerous. Conventional converter topologies become impractical due to high switching and gating losses [1]. Furthermore, it becomes increasingly difficult to implement high-side drivers, imposing additional limitations on converter topology selection. In recent publications, zero-voltage-switching (ZVS) converters with ground-referenced switches were almost exclusively used [2]–[8]; the only exceptions are low-voltage applications and converters-on-chip [9].

Switching losses in power semiconductor devices (discharge of the transistor parasitic output capacitance through the transistor on-resistance in a hard-switched design as well as current-voltage overlap during rise and fall times of the switching device) increase rapidly with frequency, thereby significantly reducing overall efficiency. Furthermore, parasitic reactive components cannot be ignored, since their sizes are comparable with the low capacitances and inductances resulting from the high frequency design. Commercial gate drivers for operation at VHF are rare; the fastest solution was introduced by IXYS for operation up to 45 MHz [10]. However, this driver is relying on hard-switching of the MOSFET gate, introducing significant gating loss. Therefore, no efficient readily available gate driver IC solution exists. To obtain gate-driving signals, VHF converters today are either oscillator-driven [3], [11] or self-oscillating [12], [13].

With the exception of the Φ_2 inverter [14] and the resonant boost converter from [5], ZVS topologies typically used today are derived from or related to class E amplifier. As a consequence, the switches are exposed to high voltage stress, typically 3.6 to 4 times the input voltage at 50% duty cycle [15]. This limits the selection of the switching devices to those with high voltage rating, which implies either higher parasitic capacitances or higher on-resistance compared to a low-voltage components. In either case, worse performance and higher losses are expected. Converters based on Φ_2 inverter require additional passive components in the resonant tank, which increases the converter size and complexity and increase the conduction losses. The resonant VHF boost converter is more space/component-efficient, and the voltage stress is the same as in the conventional boost, but it is only able to step-up the input voltage; therefore is not suitable for applications where step-down voltage conversion is required.

Recently, a method for achieving self-oscillating operation of two interleaved converters has been developed [7], [16], which addresses the gate signal generation with low component count, but the voltage stress was still 3 times the input voltage. This paper presents a modification of the interleaved self-oscillating resonant SEPIC converter [16] where the converter inputs are connected in series. Compared to the parallel-input parallel output converter, the voltage stress is reduced by a factor of two, while the voltage transformation ratio is increased by the same factor for the same output power and switching frequency. This allows a wider selection of switching devices for a given input voltage, since the breakdown voltage handling capability requirement is reduced. Furthermore, it is possible to obtain galvanic isolation between the input and the output of the converter. Only a few additional passive components in the circuit are required. Section II introduces the circuit topology and operation principle. Section III presents experimental results from a designed prototype. Section IV discusses the design considerations and challenges. Finally, section V concludes the paper.

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II. Circuit Operation

Fig. 1 shows the topology of the proposed converter. Two resonant SEPIC converters [2] are capacitively coupled together, so the drain voltage of one MOSFET is used to drive the gate of the other MOSFET. Therefore, the converters operate with a phase-shift of 180° (interleaved operation). The oscillations are started automatically when the bias voltage is increased above threshold voltage (self-oscillating operation) [7], [16]. If the power stages are identical, the input voltage is shared equally between the inverter stages. The inverters are capacitively coupled to the rectifier stages via $C_{IF} - C_{IR}$ capacitor pairs. C_{IR1} and C_{IR2} are bulk capacitors, providing DC blocking and low AC impedance between the primary (input) grounds and secondary (output) ground. Therefore, the ground of the rectifiers is "floating" in respect to the ground voltage on the input side. Isolation strength is determined by the voltage rating of $C_{IF} - C_{IR}$ capacitor pairs.

As described in [16] for the parallel-input ISOR SEPIC (shown in Fig. 2), the switching frequency may be approximately determined as

$$f_S = \frac{1}{2\pi\sqrt{L_I\, C_{DS,tot}}} \tag{1}$$

where $C_{DS,tot}$ is the total drain capacitance seen by a switch when the rectifier is shorted:

$$C_{DS,tot} = C_{DS} + C_{GD} + C_I + \frac{C_1\,(C_{GS} + C_2)}{C_1 + C_{GS} + C_2} \tag{2}$$

In Fig. 3, typical waveforms of the proposed converter are presented. Gate voltages v_{GS1} and v_{GS2} are scaled versions of v_{GS2} and v_{GS1} voltage, respectively, by a factor defined by the capacitive voltage divider; DC values of v_{GS1} and v_{GS2}

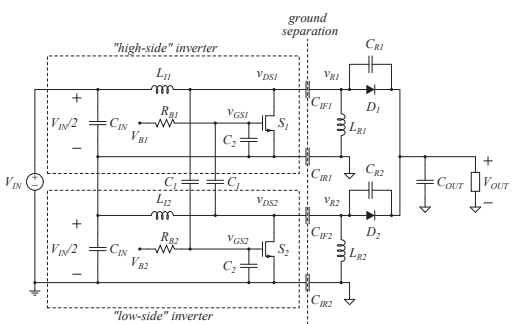


Fig. 1: Schematic of the interleaved self-oscillating resonant (ISOR) SEPIC converter with series input and parallel output (SIPO), and galvanic isolation between the inverter and the rectifier stages. "High-side" and "low-side" inverters share the input voltage. The stages are coupled via the same capacitive network as in a standard ISOR SEPIC converter.

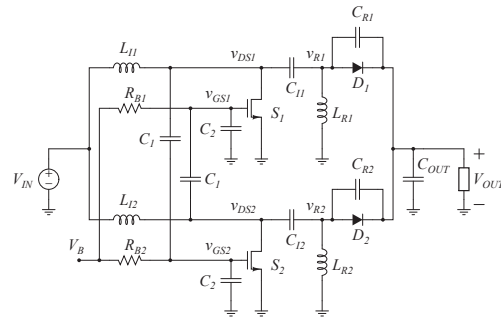


Fig. 2: Schematic of the (parallel-input parallel-output) ISOR SEPIC converter, which does not have galvanic isolation between the input and the output.

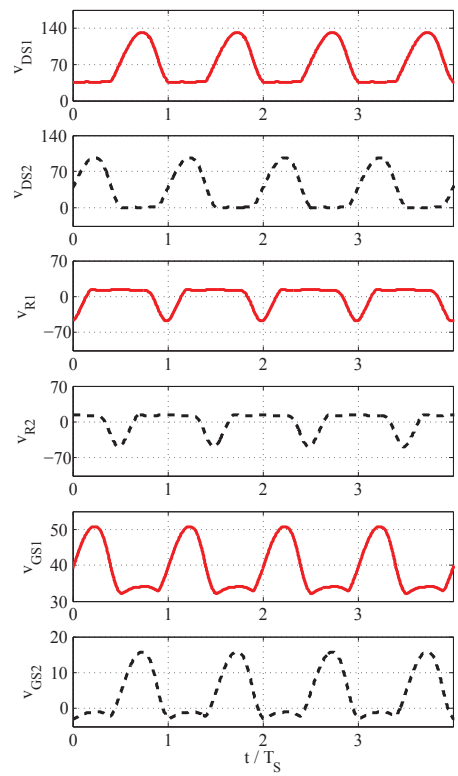


Fig. 3: Simulated waveforms of the drain, rectifier, and gate voltages of the SIPO ISOR SEPIC converter with respect to ground at the input. $V_{IN} = 70$ V and $V_{OUT} = 12$ V. Time scale is normalized to the switching period T_S.

set by V_{B1} and V_{B2}, respectively:

$$v_{GSi}(t) = V_{Bi} + v_{DSj,ac}(t)\,\frac{C_1}{C_1 + C_2 + C_{GS} + C_{GD}} \quad (3)$$
$$i, j = \{1, 2\}$$

Initial input voltage distribution between the converters may be set by a pair of balancing resistors or evening out the current consumption in the biasing circuits.

III. Experimental Results

To verify the proposed design, a proof-of-concept prototype was experimentally evaluated. The converter operation parameters are shown in Table I. Components used in the prototype are standard, low-cost semiconductor devices and passives. Capacitors in the resonant tank are 5% tolerance C0G ceramics. A complete component list is provided in Table II. Values for parasitic capacitances of the MOSFET are taken from the datasheet: $C_{GS} = 100$ pF, $C_{DS} = 21$ pF, and $C_{GD} = 7$ pF. Due to nonlinear nature of C_{DS} and C_{GD} and their dependence on v_{DS}, representative values of these capacitances are taken at the average value of v_{DS}, which is V_{IN}. With the listed components, from (1) the switching frequency is calculated as

$$f_S = \frac{1}{2\pi\sqrt{150\text{ nH}\,(22\text{ pF} + 7\text{ pF} + 66\text{ pF} + 21\text{ pF})}} \quad (4)$$
$$= 38.15\text{ MHz}$$

The achieved converter switching frequency was 37.2 MHz, which is a 2.6% error from the value predicted by (1). Efficiency of 82% was obtained for a 12 W output power; the power loss is mainly contributed by the conduction loss in the input inductor and the switch due to low Q-factor at the operating frequency, and the high on-resistance of the MOSFET.

Measured waveforms of the important voltages in the converter are shown in Fig. 5. All measurements were obtained with the oscilloscope probe connected in series with a small capacitance; therefore, the presented waveforms are scaled-down versions of the real voltages, with removed DC value. The reason for doing so is to reduce the influence of the probe on the converter operation due to impedance imbalance between d_1 and d_2. A 2.2 pF capacitance was used in for drain and rectifier voltages, and 10 pF for the gate voltage measurements. This introduces scaling factors of 0.18 and 0.51 in the respective waveforms for a 9.5 pF passive oscilloscope probe.

High-frequency ringing is observed on top of the shown voltage waveforms, caused by the parasitic inductances of the components and the layout; especially the rectifier and the gate voltages are affected. Simulations in Spice suggest that the ringing in the rectifier while the diode is ON is due to the diode parasitic inductance, which resonates with C_I when the switch is ON, and C_I in series with equivalent drain-source capacitance C_{DS}. Similar effect holds for the stray inductance in the MOSFETs with C_I and C_R. The the gate signal ringing is caused by a superposition of two effects: gate parasitic inductance ringing with the gate capacitance, and the insertion of the ringing from the power stage through C_1 and C_{GD}.

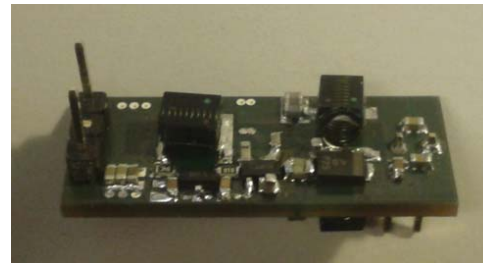


Fig. 4: Photograph of the experimental prototype.

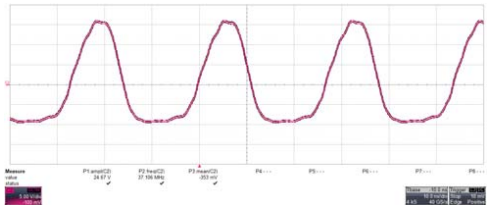
TABLE I: Converter operation parameters.

input voltage V_{IN}	70 V
output voltage V_{OUT}	12 V
output power P_{OUT}	12 W
switching frequency f_S	37.20 MHz

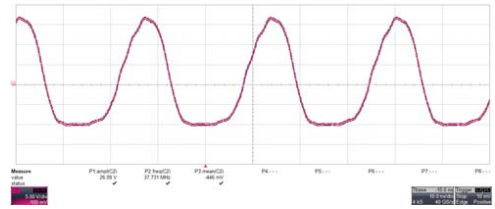
TABLE II: List of the converter components.

Component	Value
L_{I1}, L_{I2}	Coilcraft 150 nH
L_{R1}, L_{R2}	Coilcraft 150 nH
C_{I1}, C_{I2}	66 pF (C0G)
C_{IR1}, C_{IR2}	780 pF (C0G)
C_1	27 pF (C0G)
C_2	–
C_{IN}	9.4 uF (X7R)
C_{OUT}	9.4 uF (X7R)
S_1, S_2	IR IRF5802
D_1, D_2	NXP PMEG6010

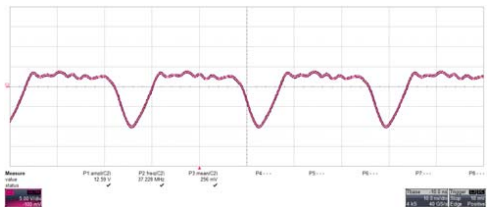
Due to imperfect matching between the components, the mid-point voltage between the converters was 33.5 V instead of intended 35 V when V_{B1} and V_{B2} are generated with biasing resistors. The reason is that the power stage with lower input voltage will have a lower bias voltage as a consequence, which further results in lower output power. Still, the converter shows a reasonably good self-balancing with no external intervention. When the biasing circuit is implemented with voltage references (VRs) in series with resistors, as shown in Fig. 6, the mid-point voltage increases to 35.5 V, thereby reducing the input voltage difference below 1.5%. The resistors in series to VRs are used to reduce the



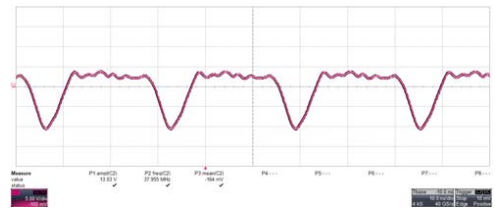
(a) v_{DS1}: 5 V/div, 10 ns/div, scaling factor 0.18



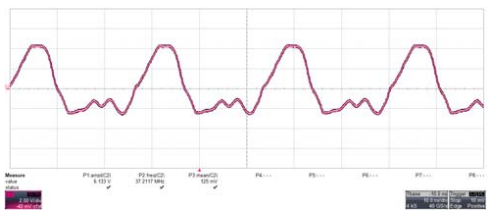
(d) v_{DS2}: 5 V/div, 10 ns/div, scaling factor 0.18



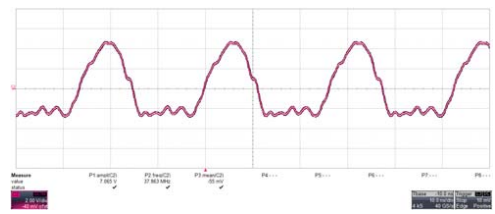
(b) v_{R1}: 5 V/div, 10 ns/div, scaling factor 0.18



(e) v_{R2}: 5 V/div, 10 ns/div, scaling factor 0.18



(c) v_{GS1}: 2 V/div, 10 ns/div, scaling factor 0.51



(f) v_{GS2}: 2 V/div, 10 ns/div, scaling factor 0.51

Fig. 5: Experimental waveforms of the 35.3 MHz, 70 V input converter. The measurements were performed with small capacitances in series with the measurement probe to reduce the influence of the probe capacitance on the circuit operation.

power consumption of the references and to postpone the turn-on of the converter until the input voltage reaches 70 V.

IV. Discussion

If the converters are ideally matched, the input voltage is shared equally between the converters. In practical implementation, the matching is never ideal and imbalance will appear in a certain degree. There are three main contributors to the imbalance in the proposed converter: asymmetry in the circuit layout, component variations, and difference in the gate bias voltages.

In order to suppress the imbalance, the converter layout has to be carefully designed. In the implementation described in this work, the layout is axially symmetrical (see Fig. 7), dictated by the pin placement of the switches. The components need to be chosen with tight tolerances. To improve capacitance matching, two or three capacitors may be used instead of one in order to reduce the equivalent series inductance and average the deviation from the desired value. This is particularly important for the gate-driving interconnection network as it influences amplitude of v_{GS1} and v_{GS2}. Use of C0G/NP0 capacitors is recommended in order to suppress the voltage and

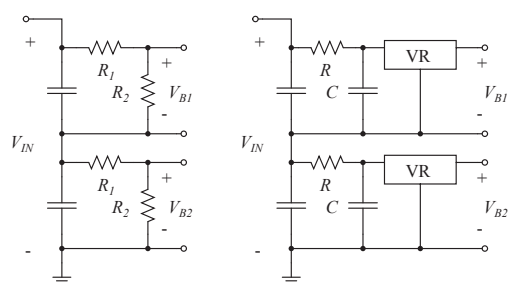


Fig. 6: Biasing circuits: passive with resistors (left) and with voltage references (right).

temperature dependence on the circuit capacitances, as well as for their high-frequency performance [17]. To further reduce variations in the converter components, as well as to increase power density of the converter, inductors may be implemented in the PCB [18].

The output power does not vary significantly with the gate

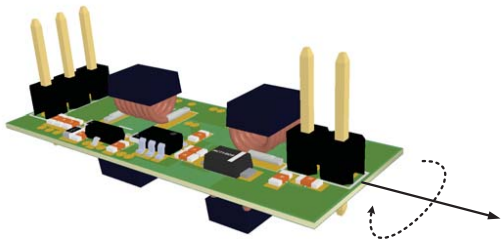


Fig. 7: Axial symmetry of the layout and component placement on the PCB.

bias voltage. However, a difference will appear if $V_{B1} \neq V_{B2}$. The most simple way to obtain V_{B1} and V_{B2} is by two pairs of biasing resistors. However, it does not guarantee equal input voltage sharing between the converters. Therefore, 5 V linear regulators are used to provide the bias voltages for the MOSFET gates, which has reduced the voltage imbalance between the converter inputs below 1.5%.

VHF converters are typically regulated using burst-mode [2]–[4] and bias voltage modulation control [5]. The interleaved converter does not show significant variation at the output with modulation of the bias voltage, therefore the converter output regulation may be obtained by implementing the burst-mode control scheme for wide load range. A mechanism for turning the "high-side" and "low-side" MOSFETs on and off needs to be provided. It is however significantly easier compared to topologies which utilize true high-side switches. The implementation of the control scheme is a subject of ongoing research.

Stacking of the inverter stages in series is not limited to 2. Each inverter may be used to drive additional inverters. The practical limitation is that the equivalent drain-source capacitance increases with each inverter stage. As a result, C_{IF} needs to be increased to maintain ZVS operation [16]. Moreover, from (1) it may be concluded that f_S will also be reduced. To maintain f_S, input inductance needs to be reduced in value, which as a consequence results in more power per converter stage. The complexity of the control circuitry also increases, as more outputs are required in the gate driver.

V. Conclusion and Future Work

In this paper, the series-input parallel-output configuration of the interleaved self-oscillating resonant SEPIC topology was introduced. This topology allows a reduction of the switch voltage stress and increases the voltage transformation ratio by a factor of two compared to the parallel-input parallel-output ISOR SEPIC converter. This is achieved using a very small number of standard, low-cost components. Upsides and downsides of the presented converter are discussed, and guidelines for circumventing them are proposed. Due to non-ideal matching between the converters, additional effort is required to obtain ideal voltage balance between the converters. Proposed solution resulted in less than 1.5% in voltage difference between the input stages. Measured waveforms of a 70 V input, 35 MHz converter were provided, reaching efficiency of 82%. As a part of the ongoing research, output regulation scheme is to be implemented. Inductors may be printed on the PCB to further increase power density and performance repeatability of the circuit.

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Appendix H

Input-Output Rearrangement of Isolated Converters

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Input-Output Rearrangement of Isolated Converters

Mickey P. Madsen*, Milovan Kovacevic*, Jakob D. Mønster*,
Jeppe A. Pedersen*, Arnold Knott*, Michael A. E. Andersen*
*Technical University of Denmark
Ørsteds Plads, building 349
2800 Kongens Lyngby
Denmark
Email: {mpma, mikov, jdomo, jarpe, akn, ma}@elektro.dtu.dk

***Abstract*— This paper presents a new way of rearranging the input and output of isolated converters. The new arrangements possess several advantages: increased voltage range, higher power handling capabilities, reduced voltage stress, and improved efficiency. The proposed approach is intended for applications where galvanic isolation is not a requirement, and is particularly valuable in power conversion at very high frequencies. Moreover, it may be combined with other stress reduction methods. Finally, the new arrangements are experimentally verified both on off the shelf converters and on a VHF resonant SEPIC converter, and results are in good agreement with the theory.**

I. Introduction

Constant strive for cost and size reduction of power converters, as well as better performance, results in higher and higher switching frequencies. From converter size and cost perspective, higher frequencies are desirable since energy storage requirements drop linearly with frequency, even though the components size and price do not typically scale at the same rate. An added benefit is cost and size reduction of filtering components. Recent advances in switching devices technology [1] and magnetic materials [2], [3] allowed converter operation in low-MHz range with high efficiencies [4]–[7]. If the switching frequency is pushed beyond 30 MHz, class E derived topologies - class E, resonant boost, resonant SEPIC, etc. - made it possible to use air-core magnetics, which eliminates core loss mechanism entirely [8], [9].

However, loss mechanisms in the switches start to dominate the total loss budget at higher frequencies. In low-MHz range, switching loss already gives incentive for use of resonant transition or quasi square-wave converter topologies (boost [10], inverted buck [6], flyback [11]). For operation above 30 MHz, switching losses impact converter efficiency so severely that only ZVS (zero voltage switching) topologies become practical. Even then, gating loss needs to be accounted for, regardless of the gating technique: hard-gating, single-resonant, or multi-resonant [12]. Needless to say, proper utilization of the switching components, especially in price-sensitive applications, is a must.

Class E derived converters exhibit voltage stress on the inverter switch of typically between 2.5 and 3.6 times input voltage, depending on the switch duty cycle [13]. As a consequence, devices with high voltage ratings are required. These devices typically perform worse compared to their lower voltage counterparts, as voltage rating comes at the expense of increase in $R_{DS,on}$ with all other parameters held the same. It is therefore of interest to reduce switch voltage blocking requirement in order to improve performance.

Voltage stress in these converters can be reduced by employing multi-resonant networks, either transmission line [14] or discrete with limited number of harmonics [15]–[17]. By implementing these techniques, switch voltage stress in VHF converters can be reduced to 2-2.5 times input voltage for the same duty cycle, but this technique requires extra resonant elements. Another approach infers single switch quasi square-wave converter topologies. The downside of quasi square-wave converters is limited converter transformation ratio (inverted buck, boost), or excessive ringing on the primary switch due to leakage inductance (flyback). In [18] a self-oscillating drive method was used to obtain a VHF self-oscillating DE inverter, in which the switch voltage stress is limited to input voltage. Finally, converter cell stacking [19], [20] reduces the switch voltage stress by N compared to a single cell case, where N is the number of converter cells. However, control becomes more complicated since it is required to balance voltages across the cells, and certain start-up issues may occur.

This paper presents a voltage stress reduction method, which may be used in either step-up or step-down applications where galvanic isolation is not a requirement. In addition to voltage stress reduction, it results in higher converter efficiency with minimum adjustments to the original circuit. Section II describes the method in detail. Section III shows experimental results when the principle is applied to conventional off-the-shelf design and a VHF prototype, respectively. Finally, Section IV concludes the paper.

II. The basic principle

Fig. 1 shows the conventional input-output configuration of an isolated dc/dc converter. If two isolated converters have their inputs connected in parallel and outputs connected in series, we obtain the structure in Fig. 2 (top). Similarly, if the inputs are connected in series and outputs in parallel, the structure in Fig. 3 (top) is obtained. Let us assume that one of the converters in each configuration is with 1:1 voltage transformation ratio. In such case, it is possible to connect its input to its output directly and remove 1:1 converter from the

circuit, without effecting the rest of the system. In doing so, part of the delivered power flows directly from input to the output, and is not processed by the converter. As a consequence, higher converter efficiency is achieved. Moreover, compared to the single cell design, voltage and/or current stresses on the switches are reduced. The only difference is that the input is not galvanic isolated from the load. Fig. 2 and 3 (bottom) demonstrate the final connection rearrangement to obtain step-up and step-down configuration, respectively.

To quantify the benefits from the proposed configurations, we analyze the case where input voltage V_{in} and output voltage V_{out} are held constant across all configurations. Moreover, output current I_{out} and output power P_{out} are held constant as well. A distinction is made between the power processed by the converter P_C, and P_{out}.

Voltage transformation ratio of the conventional converter is

$$M = \frac{V_{out}}{V_{in}} \tag{1}$$

In step-up and step-down configurations, transformation ratio of the converter cell only becomes

$$M_{up} = \frac{V_{out} - V_{in}}{V_{in}} \tag{2}$$

$$M_{down} = \frac{V_{out}}{V_{in} - V_{out}} \tag{3}$$

In general, switch voltage stress is a function of both input and output voltages. In step-up configuration, output voltage stress contribution is reduced by a factor of $(1 - V_{in}/V_{out})$. In step-down configuration, input voltage stress contribution is reduced by $(1 - V_{out}/V_{in})$.

Output power of all three configurations is the same:

$$P_{out} = V_{out}\ I_{out} \tag{4}$$

The power processed by the converter P_C in the conventional structure is equal to P_{out}. In the step-up and step-down cases, this power is given as

$$P_{C,up} = P_{out}\left(1 - \frac{V_{in}}{V_{out}}\right) \tag{5}$$

$$P_{C,down} = P_{out}\left(1 - \frac{V_{out}}{V_{in}}\right) \tag{6}$$

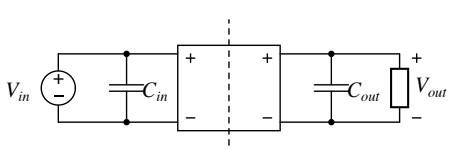


Fig. 1. Conventional isolated dc/dc converter topology. Dashed line represents galvanic isolation.

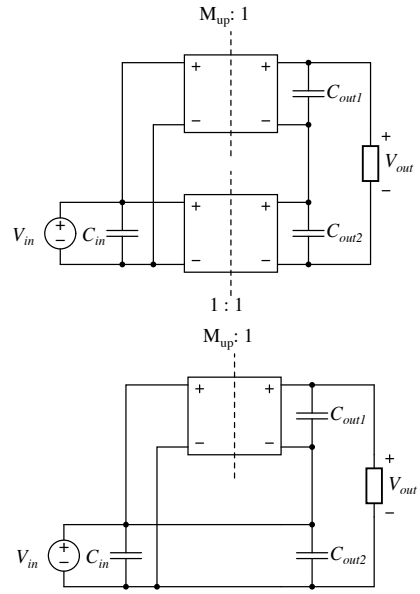


Fig. 2. Step-up configuration: two converter cells with inputs in parallel and outputs in series (top) and a single cell equivalent (bottom).

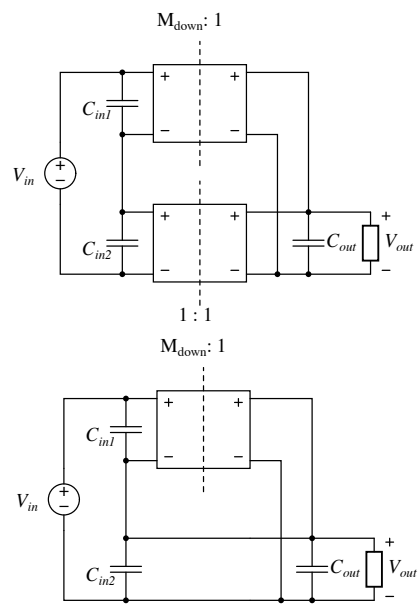


Fig. 3. Step-down configuration: two converter cells with inputs in parallel and outputs in series (top) and a single cell equivalent (bottom).

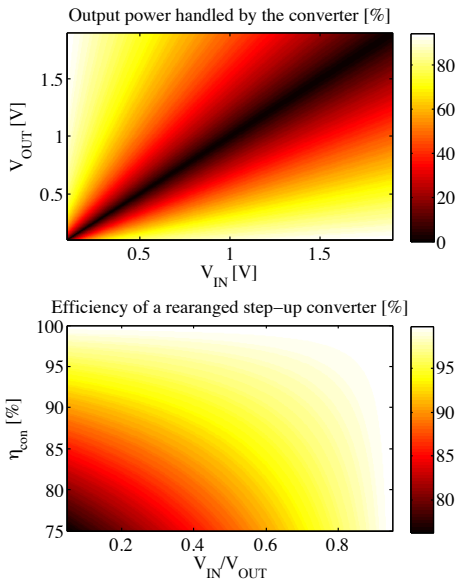


Fig. 4. Power processed by the converter and efficiency improvement by rearranging.

$P_{C,up}$ and $P_{C,down}$ are smaller than P_{out}, and the remaining power is delivered through the DC path. Efficiency of that power transfer is very close to 100%. Assuming that P_C, $P_{C,up}$, and $P_{C,down}$ are transfered with the same efficiency η, effective efficiencies of the step-up and step-down configurations can be expressed in terms of η, P_{out}, and $P_{C,up/down}$:

$$\eta_{up/down} = \eta \frac{P_{C,up/down}}{P_{out}} + \frac{P_{out} - P_{C,up/down}}{P_{out}} \quad (7)$$

Equations 5-7 are illustrated in Fig. 4. The plot clearly shows that for limited step-up or step-down ratios, the percentage of the output power processed by the converter is small and hence the efficiency improvement becomes significant. For a step-up converter with 330V input and 400V output only 17.5% of the output power would be processed by the converter and if the converter efficiency were 80%, the rearranged efficiency would be 96.5%. The converter would in that case have to be designed as an galvanic isolated converter with 330V input, 70V output and a peak output power equal to 17.5% of the required power. Hence a high power boost converter with high efficiency could be replaced by a low power flyback or SEPIC converter with moderate efficiency while achieving the same overall system performance.

Adaptations shown in Fig. 2 and 3 can be used for any type of isolated converter, regardless of the isolation type (inductive or capacitive). In Fig. 5, a flyback converter is used in a step-up configuration, along with simulated waveforms. Fig. 6 presents

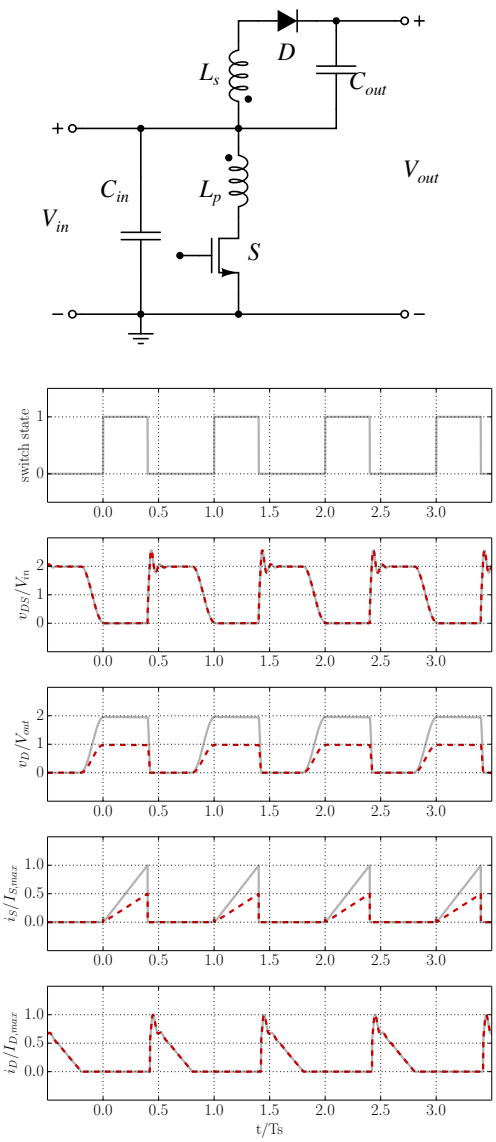


Fig. 5. Flyback converter in step-up configuration (top) and simulated waveforms of a quasi square-wave 1:2 flyback converter in conventional (solid black) and step-up (dashed red) configuration. Diode voltage and switch current stresses are reduced by a factor of 2. Output capacitance is formed by series connected C_{out} and C_{in}.

a class DE converter (DE inverter and DE rectifier) in step-down configuration.

The proposed technique may be used together with multi-

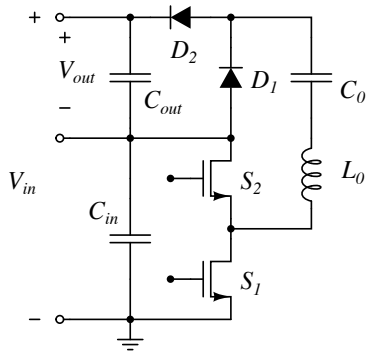


Fig. 6. Class DE converter in step-down configuration with output referenced to the inverter input. Parasitic capacitances of the switching devices are included implicitly.

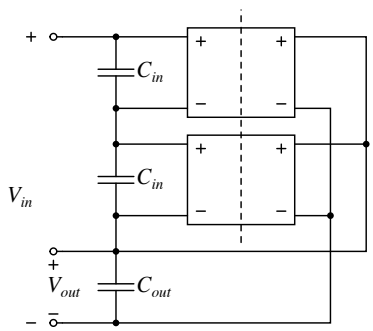


Fig. 7. Two stacked converters in step-down configuration.

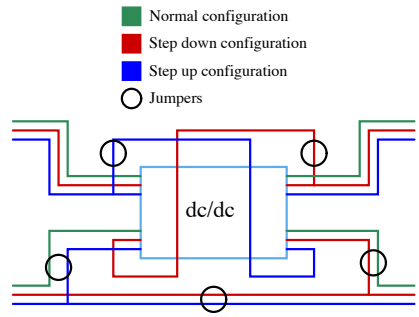
cell stacked designs, as shown in Fig. 7. This also adds complexity to control circuitry since it needs to monitor and balance voltages across the cells.

III. Experimental Results

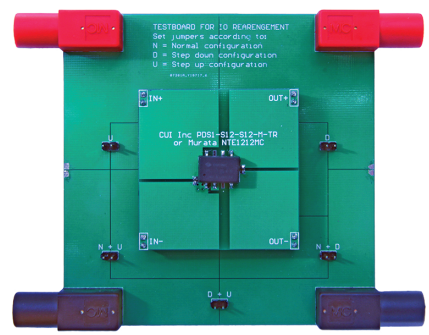
A. Off the shelf converter

In order to experimentally verify equation 5-7 a test setup with two isolated 12-12V DC/DC converters (Murata NTE1212MC and CUI Inc PDS1-S12-S12-S) has been made. The setup is made with five jumpers allowing the setup to be changed between normal configuration (12-12V), step down (24-12V) and step up (12-24V).

The measured efficiency as function of output power is shown in Fig. 9. The increased efficiency and power handling capability in the new configurations are clearly seen. With a 1-2 or 2-1 step ratio the converter only handles 50% of the output power (see equation 5-6). The power handling capability is hence doubled while the efficiency is increased across the entire load range with half the loss at full load.



(a) Schematic



(b) PCB

Fig. 8. Test board for evaluation of the principle.

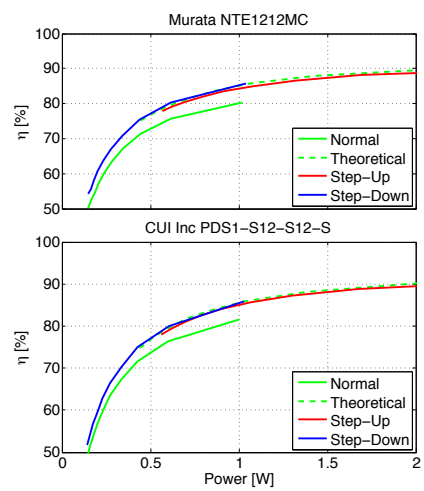


Fig. 9. Performance improvements of two rearranged converters.

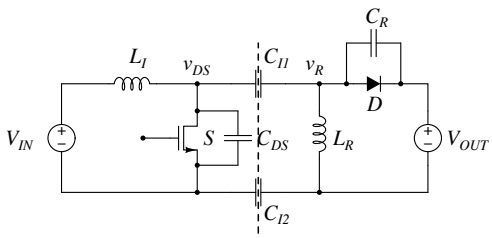


Fig. 10. Resonant SEPIC converter with capacitive galvanic isolation.

B. Resonant SEPIC converter

As mentioned in Section I, the input and output voltage and the subsequent voltage stress on the semiconductors is of high importance in resonant converters. The availability of suitable semiconductors is reduced significantly as the break down voltage requirement gets above 100 V. Furthermore the amount of resonating current needed in order to achieve zero voltage switching scales with the voltage squared, hence a reduction in input and output voltage will lead to significantly lower currents and thereby also reduced losses due to ESR in the components.

As the switching loss in resonant converters with ZVS is reduced to a minimum, these converters are operable at several tens of MHz [12], [15]–[19], [21]–[32]. At these frequencies, galvanic isolation can be achieved simply by adding a small capacitor in the return path between the inverter and rectifier.

The proposed rearrangement is hence extremely well suited for non-isolated converters where very high frequency resonant converters can be used to achieve high power density, low cost and weight and still keep the efficiency high. In order to show the benefit in these type of converters a resonant SEPIC converter (see Fig. 10) switching at 50 MHz has been implemented and tested on the test board in Fig. 8.

Figure 11 shows the performance improvements measured with this setup. From the plot it is clearly seen that both the efficiency and the voltage and power handling capability are increased. The measurements and theoretical values for the step down version fits well as the loading conditions as well as the input voltage are the same. For the step-up version the output voltage from the converter changes quite dramatically as the input voltage is increased and becomes close to zero towards the end.

In [18] the same principle is shown for a capacitively isolated VHF class DE converter. Here the rearangement increases the efficiency by 5-10% across a wide input voltage range. At the same time the input voltage and output power is increased by approx 50%.

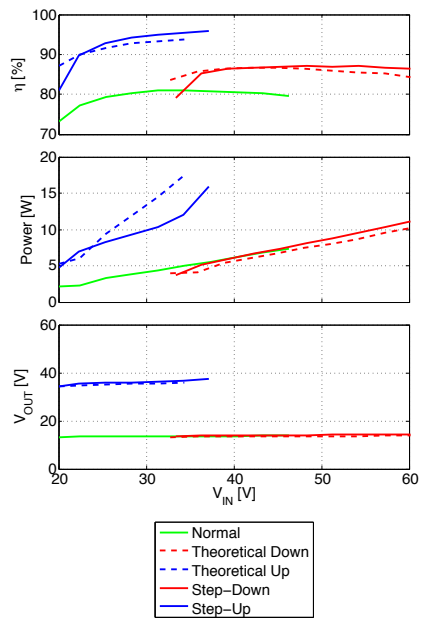


Fig. 11. Performance improvement of a VHF resonant SEPIC.

IV. Conclusion

The paper presents a voltage and/or current stress reduction technique for isolated dc-dc converters in applications where isolation is not a requirement. The technique provides higher efficiency compared to a conventional single cell design, and it can be combined with other methods of voltage stress reduction, as long as the initial converter provides capacitive or inductive isolation. Obtained benefits are considered very appealing for certain non-isolated applications, such as LED lighting. Theoretical analysis and experimental results are provided and are in good agreement.

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Department of Electrical Engineering
Electronics Group (ELE)
Technical University of Denmark
Oersteds Plads bygning 349
DK-2800 Kgs. Lyngby
Denmark

www.ele.elektro.dtu.dk
Tel: (+45) 45 25 25 25
Fax: (+45) 45 88 01 17
Email: elektro@elektro.dtu.dk